System Module

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Transceiver NSM–1

Introduction

The NSM–1 is a dualband transceiver unit designed for operation in GSM900, GSM1800 and GSM900/1800 dualband networks. GSM power class is 4 and PCN power class is 1.

The transceiver has full graphic display, and the user interface is based on two soft keys.

The transceiver has leakage tolerant earpiece and omnidirectional microphone providing excellent audio quality. Transceiver supports full rate, enhanced full rate and half rate speech decoding.

The antenna is a fixed helix. External antenna connection is provided by rear RF connector

Integrated IR link provides for connection between two NSM–1NY transceivers or a transceiver and a PC, or a transceiver and a printer.

The small SIM (Subscriber Identity Module) card is located inside the phone, beneath the battery pack.

Mode Description

There are five different operation modes:

– power off mode

– idle mode

– active mode

– charge mode

– local mode

In the power off mode only the circuits needed for power up are supplied.

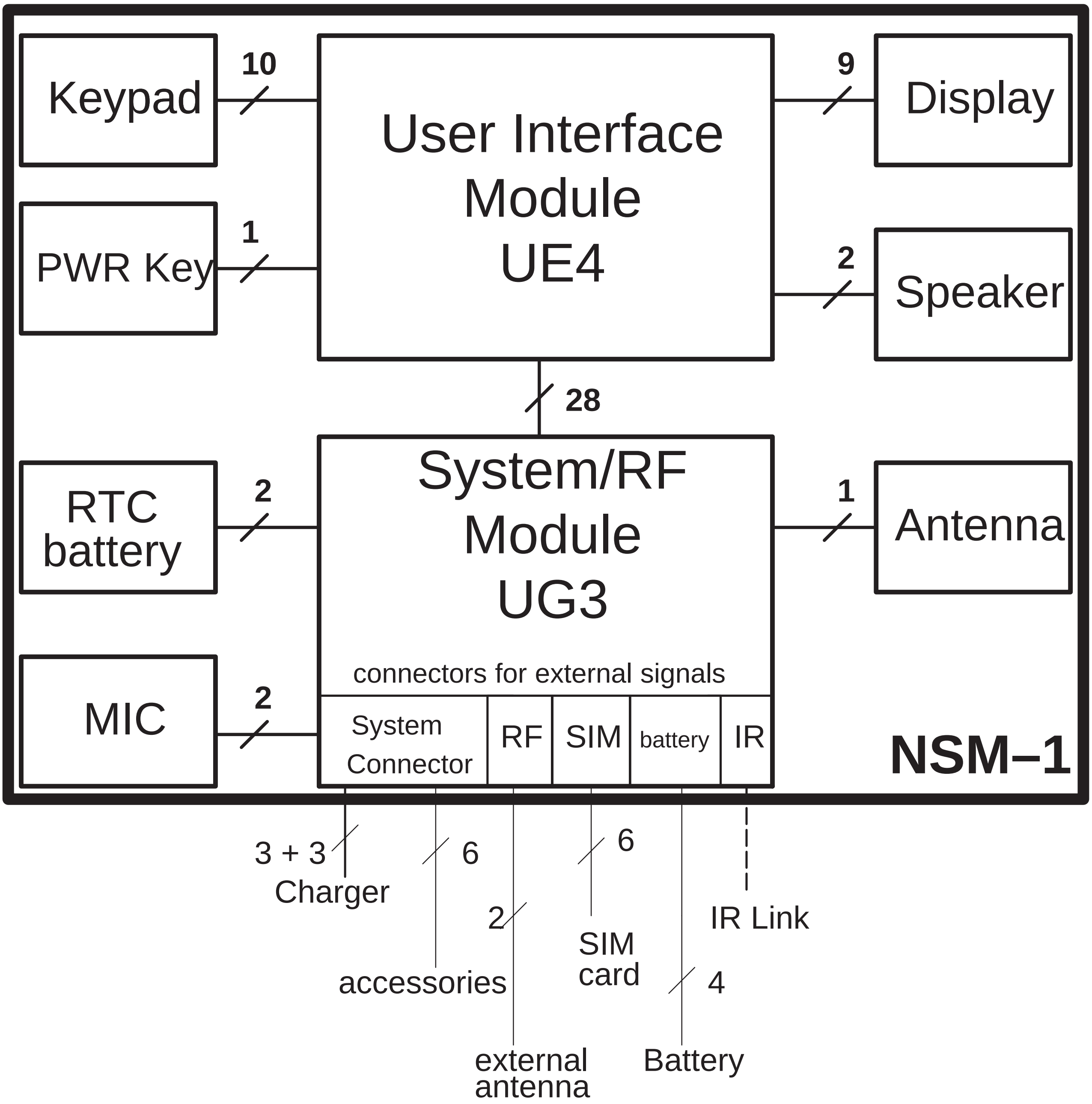
In the idle mode circuits are powered down and only sleep clock is running.

In the active mode all the circuits are supplied with power although some parts might be in the idle state part of the time.

The charge mode is effective in parallel with all previous modes. The charge mode itself consists of two different states, i.e. the charge and the maintenance mode.

The local mode is used for alignment and testing.

Interconnection Diagram



System Module

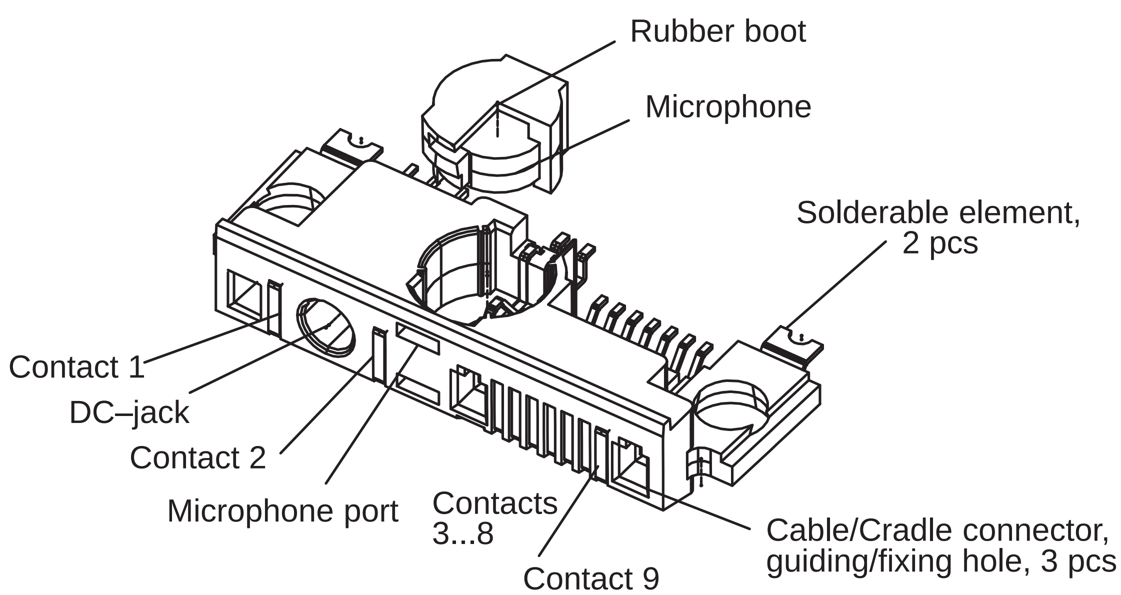
Circuit Description

The transceiver electronics consist of the Radio Module, RF + System blocks, the UI PCB, the display module and audio components. The keypad and the display module are connected to the Radio Module with a connectors. System blocks and RF blocks are interconnected with PCB wiring. The Transceiver is connected to accessories via a bottom system connector with charging and accessory control.

The System blocks provide the MCU, DSP and Logic control functions in MAD ASIC, external memories, audio processing and RF control hardware in COBBA ASIC. Power supply circuitry CCONT ASIC delivers operating voltages both for the System and the RF blocks.

The RF block is designed for a handportable phone which operates in the GSM and DCS1800 systems. The purpose of the RF block is to receive and demodulate the radio frequency signal from the base station and to transmit a modulated RF signal to the base station. The SUMMA ASIC is used for VHF and PLL functions. The CRFU3 ASIC is used at the front end.

External and Internal Connectors



System Connector Contacts

Con-tact	Line Sym-bol	Parameter	Mini-mum	Typical / Nomi-nal	Maxi-mum	Unit / Notes
1	VIN	Charger input voltage Charger input current	7.1 720 7.24 320	8.4 800 7.6 370	9.3 850 7.95 420	V/ Unloaded ACP–9 Charger mA/ Supply current V/ Unloaded ACP–7 Charger mA/ Supply current
DC–JACK	L_GND	Charger ground input	0	0	0	V/ Supply ground
DC–JACK	VIN	Charger input voltage Charger input current	7.1 720 7.24 320	8.4 800 7.6 370	9.3 850 7.95 420	V/ Unloaded ACP–9 Charger mA/ Supply current V/ Unloaded ACP–7 Charger mA/ Supply current
DC–JACK	CHRG CTRL	Output high voltage PWM frequency	2.0	32	2.8	V/ Charger control (PWM) high Hz /PWM frequency for charger
2	CHRG CTRL	Output high voltage PWM frequency	2.0	32	2.8	V/ Charger control (PWM) high Hz /PWM frequency for charger
Mic ports		Acoustic signal	N/A	N/A	N/A	Microphone sound ports
3	XMIC	Input signal voltage		60	1 Vpp	mVrms
4	SGND	Signal ground	0		0	mVrms
5	XEAR	Output signal voltage		80	1 Vpp	mVrms
6	MBUS	I/O low voltage I/O high voltage	0 2.0		0.8 2.8	Serial bidirectional control bus. Baud rate 9600 Bit/s
7	FBUS_RX	Input low voltage Input high voltage	0 2.0		0.8 2.8	V/ Fbus receive. V/ Serial Data, Baud rate 9.6k–230.4kBit/s
8	FBUS_TX	Output low voltage Output high voltage	0 2.0		0.8 2.8	V/ Fbus transmit. V/ Serial Data, Baud rate 9.6k–230.4kBit/s
9	L_GND	Charger ground input	0	0	0	V/ Supply ground

RF Connector Contacts

Contact	Line Symbol	Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
1	EXT_ANT	Impedance		50ohm		External antenna connector, 0 V DC
2	GND					

Supply Voltages and Power Consumtion

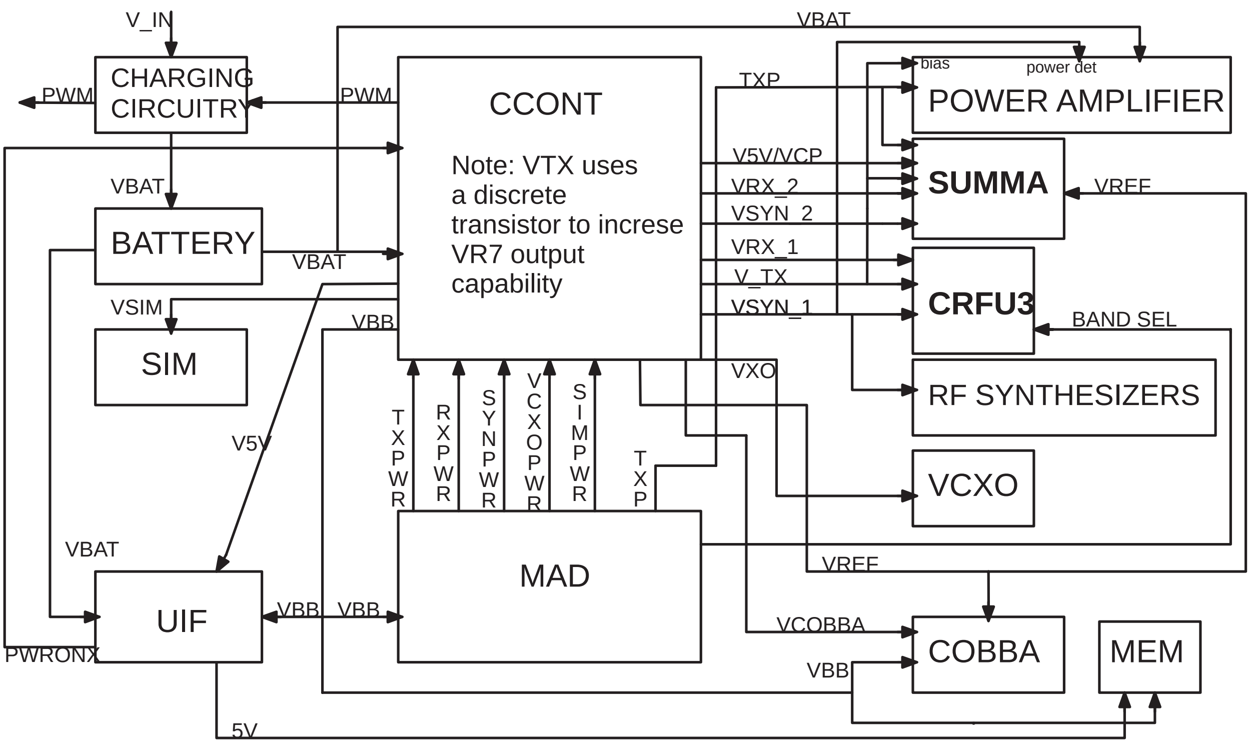
Connector	Line Symbol	Minimum	Typical / Nominal	Maximum/ Peak	Unit / Notes
Charging	VIN	7.1	8.4	9.3	V/ Travel charger, ACP–9
Charging	VIN	7.25	7.6	7.95	V/ Travel charger. ACP–7
Charging	I / VIN	720	800	850	mA/ Travel charger, ACP–9
Charging	I / VIN	320	370	420	mA/ Travel charger, ACP–7

Power Distribution Diagram

The power supply is based on the ASIC circuit CCONT. The chip consists of regulators and control circuits providing functions like power up, reset and watchdog. External buffering is required to provide more current on some blocks.

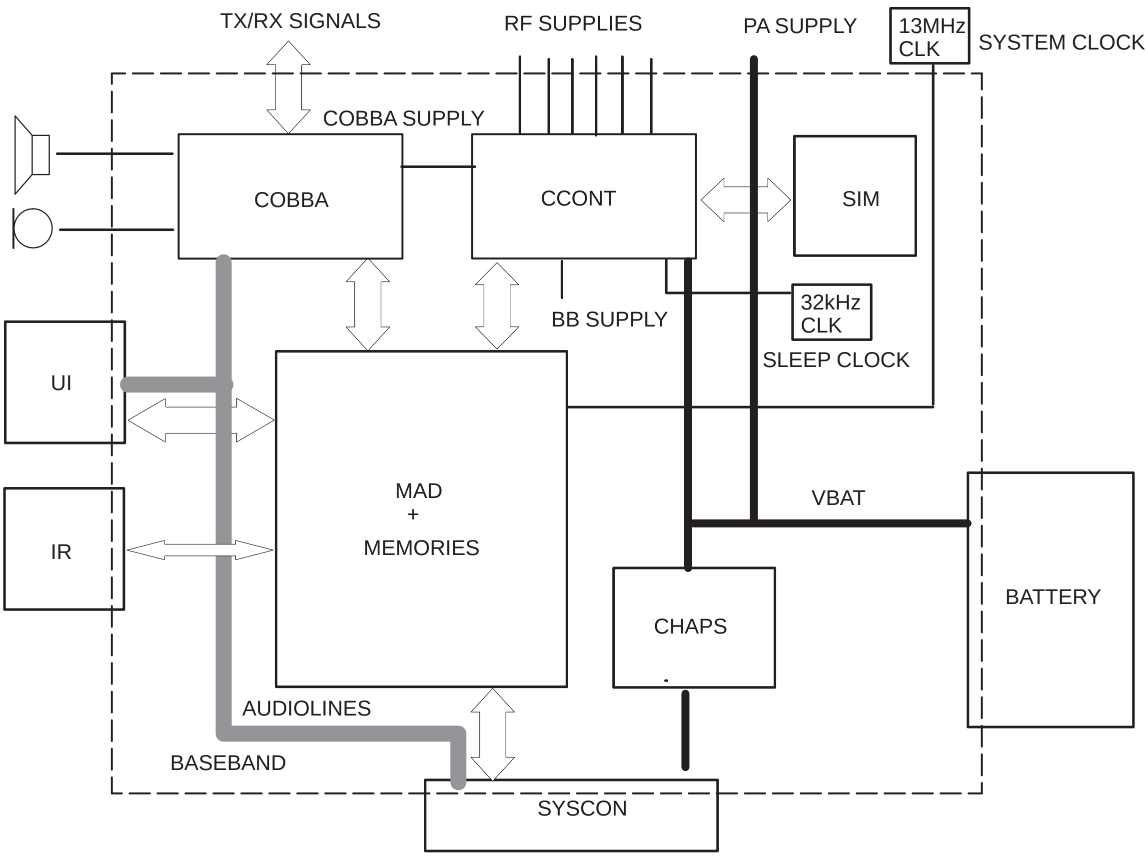
The MCU and the CCONT circuits control charging together, detection being carried out by the CCONT and higher level intelligent control by the MCU. The MCU measures battery voltage by means of the CCONT. The CCONT also measures charger voltage, temperature and size of the battery.

Detailed power distribution diagrams are given in Baseband blocks and RF blocks later in the document.



Baseband Module

Block Diagram



Technical Summary

The baseband module consists of four asics, CHAPS, CCONT, COBBA–GJ and MAD2, which take care of the baseband functions of NSM–1.

The baseband is running from a 2.8V power rail, which is supplied by a power controlling asic. In the CCONT asic there are 6 individually controlled regulator outputs for RF–section and two outputs for the baseband. In addition there is one +5V power supply output (V5V) for flash programming voltage and other purposes where a higher voltage is needed. The CCONT contains also a SIM interface, which supports both 3V and 5V SIM–cards. A real time clock function is integrated into the CCONT, which utilizes the same 32kHz clock supply as the sleep clock. A backup power supply is provided for the RTC, which keeps the real time clock running when the main battery is removed. The backup power supply is a rechargable polyacene battery. The backup time with this battery is minimum of ten minutes.

The interface between the baseband and the RF section is handled by a specific asic. The COBBA asic provides A/D and D/A conversion of the in–phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the UI section. The COBBA supplies the analog TXC and AFC signals to rf section according to the MAD DSP digital control and converts analog AGC into digital signal for the DSP. Data transmission between the COBBA and the MAD is implemented using a parallel connection for high speed signalling and a serial connection for PCM coded audio signals. Digital speech processing is handled by the MAD asic. The COBBA asic is a dual voltage circuit, the digital parts are running from the baseband supply VBB and the analog parts are running from the analog supply VCOBBA.

The baseband supports three external microphone inputs and two external earphone outputs. The inputs can be taken from an internal microphone, a headset microphone or from an external microphone signal source. The microphone signals from different sources are connected to separate inputs at the COBBA asic.

The output for the internal earphone is a dual ended type output capable of driving a dynamic type speaker. Input and output signal source selection and gain control is performed inside the COBBA asic according to control messages from the MAD. Keypad tones, DTMF, and other audio tones are generated and encoded by the MAD and transmitted to the COBBA for decoding. A buzzer and an external vibra alert control signals are generated by the MAD with separate PWM outputs.

EMC shieding is implemented using a metallized plastic B–cover with a conductive rubber seal on the ribs. On the other side the engine is shielded with a frame having a conductive rubber on the inner walls, which makes a contact to a ground ring of the engine board and a ground plane of the UI–board. Heat generated by the circuitry will be conducted out via the PCB ground planes.

Bottom Connector External Contacts

Contact	Line Symbol	Function
1	VIN	Charger input voltage
DC–jack side contact (DC–plug ring)	L_GND	Charger ground
DC–jack center pin	VIN	Charger input voltage
DC–jack side contact (DC–plug jacket)	CHRG_CTRL	Charger control output (from phone)
2	CHRG_CTRL	Charger control output (from phone)
Microphone acoustic ports		Acoustic signal (to phone)
3	XMIC	Accessory microphone signal input (to phone)
4	SGND	Accessory signal ground
5	XEAR	Accessory earphone signal output (from phone)
6	MBUS	MBUS, bidirectional serial data i/o
7	FBUS_RX	FBUS, unidirectional serial data input (to phone)
8	FBUS_TX	FBUS, unidirectional serial data output (from phone)
9	L_GND	Charger ground

Bottom Connector Signals

Pin	Name	Min	Typ	Max	Unit	Notes
1,3	VIN	7.25	7.6	7.95	V	Unloaded ACP–7 Charger (5kohms load)
				16.9	V	Peak output voltage (5kohms load)
		3.25	3.6	3.95	V	Loaded output voltage (10ohms load)
		320	370	420	mA	Supply current
		7.1	8.4	9.3	V	Unloaded ACP–9 Charger
		3.25	3.6	3.95	V	Loaded output voltage (10ohms load)
		720	800	850	mA	Supply current
2	L_GND	0		0	V	Supply ground
4,5	CHRG_ CTRL	0		0.5	V	Charger control PWM low
		2.0		2.85	V	Charger control PWM high
			32		Hz	PWM frequency for a fast charger
		1		99	%	PWM duty cycle
6	MICP		N/A			see section Internal microphone
7	MICN		N/A			see section Internal microphone

Pin	Name	Min	Typ	Max	Unit	Notes
8	XMIC	2.0		2.2	kΩ	Input AC impedance
				1	Vpp	Maximum signal level
		1.47		1.55	V	Mute (output DC level)
		2.5		2.85	V	Unmute (output DC level)
		100		600	µA	Bias current
			58	490	mV	Maximum signal level
	HMIC	0	3.2	29.3	mV	Microphone signal Connected to COBBA MIC3P input
9	SGND		47		Ω	Output AC impedance (ref. GND)
			10		µF	Series output capacitance
			380		Ω	Resistance to phone ground
10	XEAR		47		Ω	Output AC impedance (ref. GND)
			10		µF	Series output capacitance
		16		300	Ω	Load AC impedance to SGND (Head-set)
		4.7	10		kΩ	Load AC impedance to SGND (Acces-sory)
			1.0		Vpp	Maximum output level (no load)
			22	626	mV	Output signal level
			10		kΩ	Load DC resistance to SGND (Acces-sory)
		16		1500	Ω	Load DC resistance to SGND (Head-set)
			2.8		V	DC voltage (47k pull–up to VBB)
	HEAR		28	626	mV	Earphone signal (HF– HFCM) Connected to COBBA HF output
11	MBUS	0 2.0	logic low logic high	0.8 2.85	V	Serial bidirectional control bus. Baud rate 9600 Bit/s Phone has a 4k7 pullup resistor
12	FBUS_RX	0 2.0	logic low logic high	0.8 2.85	V	Fbus receive. Serial Data Baud rate 9.6k–230.4kBit/s Phone has a 220k pulldown resistor
13	FBUS_TX	0 2.0	logic low logic high	0.5 2.85	V	Fbus transmit. Serial Data Baud rate 9.6k–230.4kBit/s Phone has a 47k pullup resistor
14	GND	0		0.3	V	Supply ground

Battery Connector

Pin	Name	Min	Typ	Max	Unit	Notes
1	BVOLT	3.0	3.6	4.5	V	Battery voltage
				5.0		Maximum voltage in call state with charger
				5.3		Maximum voltage in idle state with charger
2	BSI	0		2.85	V	Battery size indication Phone has 100kohm pull up resistor. SIM Card removal detection (Treshold is 2.4V@VBB=2.8V)
		2.2		18	kohm	Battery indication resistor (Ni battery)
		20	22	24	kohm	Battery indication resistor (service battery)
		27		51	kohm	Battery indication resistor (4.1V Lithium battery)
		68		91	kohm	Battery indication resistor (4.2V Lithium battery)
3	BTEMP	0		1.4	V	Battery temperature indication Phone has a 100k (+–5%) pullup resistor, Battery package has a NTC pulldown resistor: 47k+–5%@+25C , B=4050+–3%
		2.1		3	V	Phone power up by battery (input)
		5	10	20	ms	Power up pulse width
		1.9		2.85	V	Battery power up by phone (output)
		90	100	200	ms	Power up pulse width
		0		1	kohm	Local mode initialization (in production)
		20	22	25	kHz	PWM control to VIBRA BATTERY
4	BGND	0		0	V	Battery ground

SIM Card Connector

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
4	GND	GND	0		0	V	Ground
3, 5	VSIM	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Supply voltage
6	DATA	5V Vin/Vout 3V Vin/Vout	4.0 0 2.8 0	”1” ”0” ”1” ”0”	VSIM 0.5 VSIM 0.5	V	SIM data Trise/Tfall max 1us
2	SIMRST	5V SIM Card 3V SIM Card	4.0 2.8	”1” ”1”	VSIM VSIM	V	SIM reset
1	SIMCLK	Frequency Trise/Tfall		3.25	 25	MHz ns	SIM clock

Internal Microphone

Pin	Name	Min	Typ	Max	Unit	Notes
6	MICP		0.55	4.1	mV	Connected to COBBA MIC2N input. The maximum value corresponds to1 kHz, 0 dBmO network level with input amplifier gain set to 32 dB. typical value is maximum value – 16 dB.
7	MICN		0.55	4.1	mV	Connected to COBBA MIC2P input. The maximum value corresponds to1 kHz, 0 dBmO network level with input amplifier gain set to 32 dB. typical value is maximum value – 16 dB.

Infrared Module Connections

An infrared transceiver module is designed to substitute an electrical cable between the phone and a PC. The infrared transceiver module is a stand alone component capable to perform infrared transmitting and receiving functions by transforming signals transmitted in infrared light from and to electrical data pulses running in two wire asyncronous databus. In DCT3 the module is placed inside the phone at the top of the phone.

Signal	Parameter	Min	Typ	Max	Unit	Notes
IRON	IR–module on/off	2.0		2.85	V	Iout@2mA
FBUS_RX	IR receive pulse	0		0.8	V	
	IR receive no pulse	2.0		2.85	V	
FBUS_TX	IR transmit pulse	2.0		2.85	V	Iout@2mA
	IR transmit no pulse	0		0.5	V	

RTC Backup Battery

The RTC block in CCONT needs a power backup to keep the clock running when the phone battery is disconnected. The backup power is supplied from a rechargable polyacene battery that can keep the clock running minimum of 10 minutes. The backup battery is charged from the main battery through CHAPS.

Signal	Parameter	Min	Typ	Max	Unit	Notes
VBACK	Backup battery charging from CHAPS	3.02	3.15	3.28	V	
	Backup battery charging from CHAPS	100	200	500	uA	Vout@VBAT–0.2V
VBACK	Backup battery supply to CCONT	2		3.28	V	Battery capacity 65uAh
	Backup battery supply to CCONT		80		uA	

Buzzer

Signal	Maximum output current	Input high level	Input low level	Level (PWM) range, %	Frequency range, Hz
BuzzPWM / BUZZER	2mA	2.5V	0.2V	0...50 (128 linear steps)	440...4700

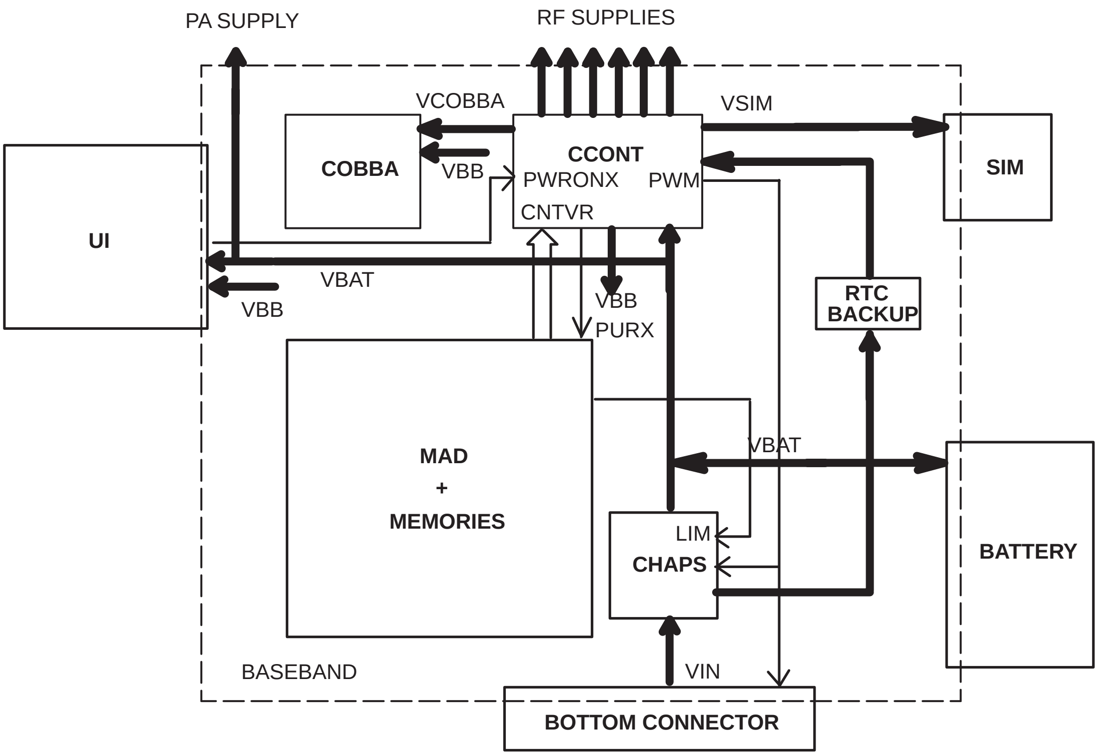
Baseband Power Distribution

Functional Description

In normal operation the baseband is powered from the phone‘s battery. The battery consists of three Nickel Metal Hydride cells. There is also a possibility to use batteries consisting of one Lithium–Ion cell. An external charger can be used for recharging the battery and supplying power to the phone. The charger can be either a standard charger that can deliver around 400 mA or so called performance charger, which can deliver supply current up to 850 mA.

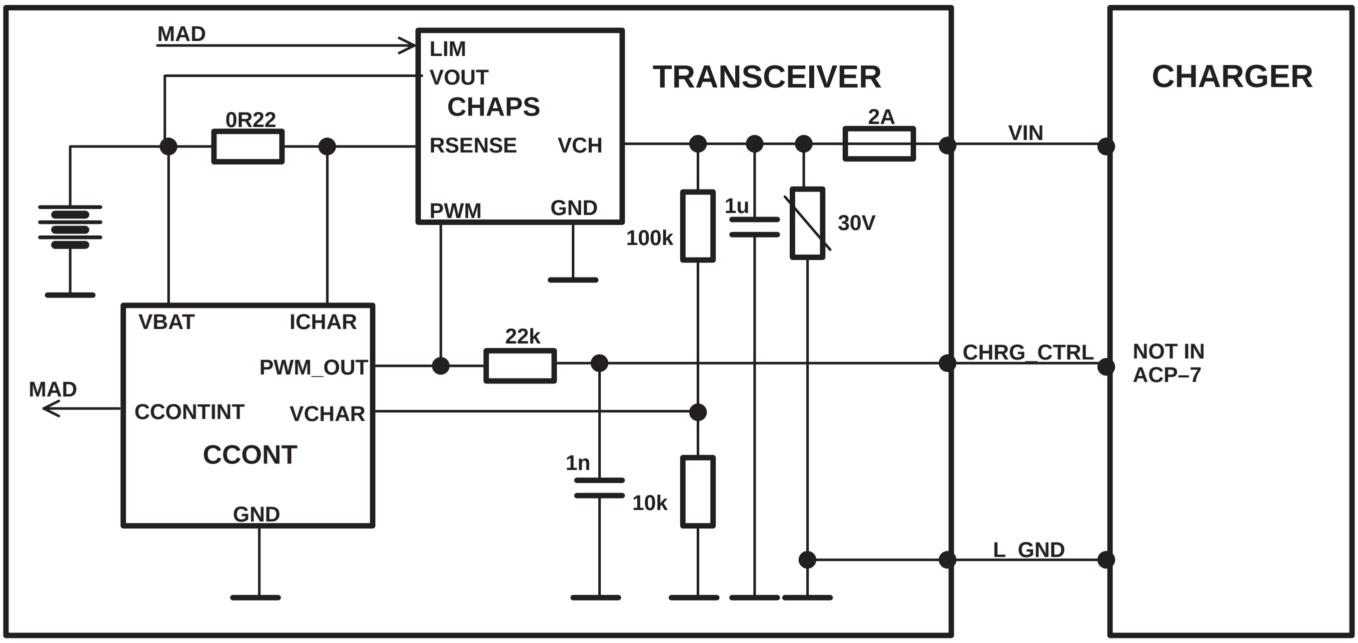
The baseband contains components that control power distribution to whole phone excluding those parts that use continuous battery supply. The battery feeds power directly to three parts of the system: CCONT, power amplifier, and UI (buzzer and display and keyboard lights). Figure below shows a block diagram of the power distribution.

The power management circuit CHAPS provides protection agains over-voltages, charger failures and pirate chargers etc. that would otherwise cause damage to the phone.



Battery charging

The electrical specifications give the idle voltages produced by the acceptable chargers at the DC connector input. The absolute maximum input voltage is 30V due to the transient suppressor that is protecting the charger input. At phone end there is no difference between a plug–in charger or a desktop charger. The DC–jack pins and bottom connector charging pads are connected together inside the phone.



Startup Charging

When a charger is connected, the CHAPS is supplying a startup current minimum of 130mA to the phone. The startup current provides initial charging to a phone with an empty battery. Startup circuit charges the battery until the battery voltage level is reaches 3.0V (+/– 0.1V) and the CCONT releases the PURX reset signal and program execution starts. Charging mode is changed from startup charging to PWM charging that is controlled by the MCU software. If the battery voltage reaches 3.55V (3.75V maximum) before the program has taken control over the charging, the startup current is switched off. The startup current is switched on again when the battery voltage is sunken 100mV (nominal).

Parameter	Symbol	Min	Typ	Max	Unit
VOUT Start– up mode cutoff limit	Vstart	3.45	3.55	3.75	V
VOUT Start– up mode hysteresis NOTE: Cout = 4.7 uF	Vstarthys	80	100	200	mV
Start–up regulator output current VOUT = 0V ... Vstart	Istart	130	165	200	mA

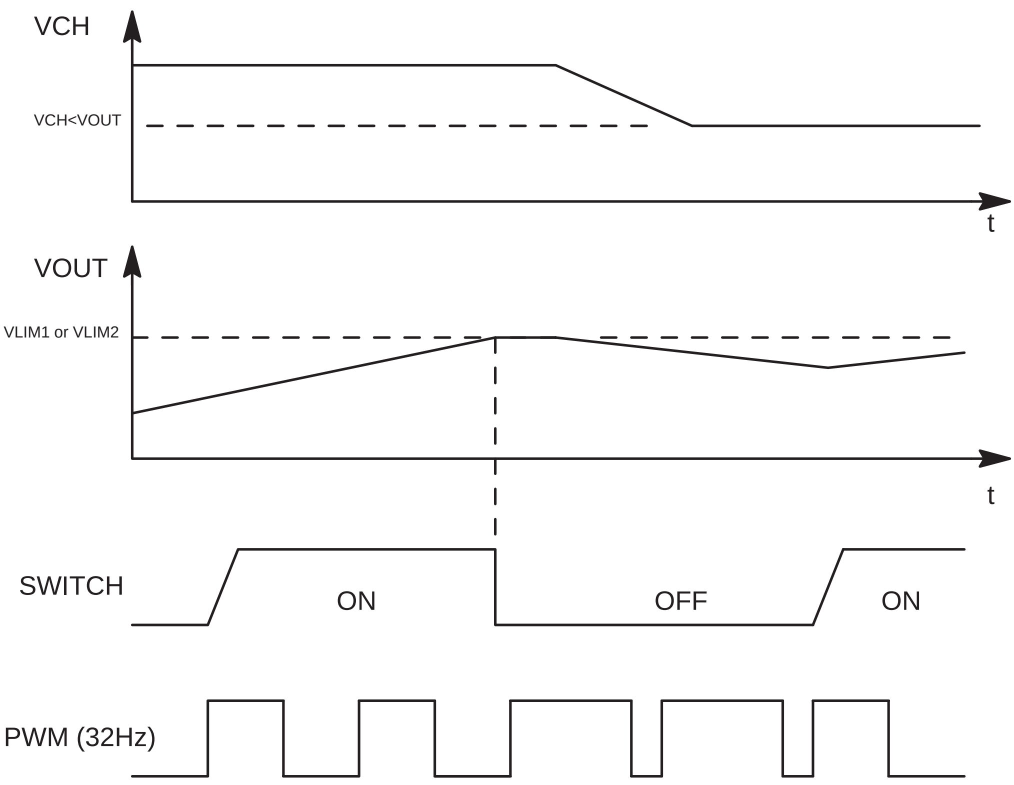
Battery Overvoltage Protection

Output overvoltage protection is used to protect phone from damage. This function is also used to define the protection cutoff voltage for different battery types (Li or Ni). The power switch is immediately turned OFF if the voltage in VOUT rises above the selected limit VLIM1 or VLIM2.

Parameter	Symbol	LIM input	Min	Typ	Max	Unit
Output voltage cutoff limit (during transmission or Li–battery)	VLIM1	LOW	4.4	4.6	4.8	V
Output voltage cutoff limit (no transmission or Ni–battery)	VLIM2	HIGH	4.8	5.0	5.2	V

The voltage limit (VLIM1 or VLIM2) is selected by logic LOW or logic HIGH on the CHAPS (N101) LIM– input pin. Default value is lower limit VLIM1.

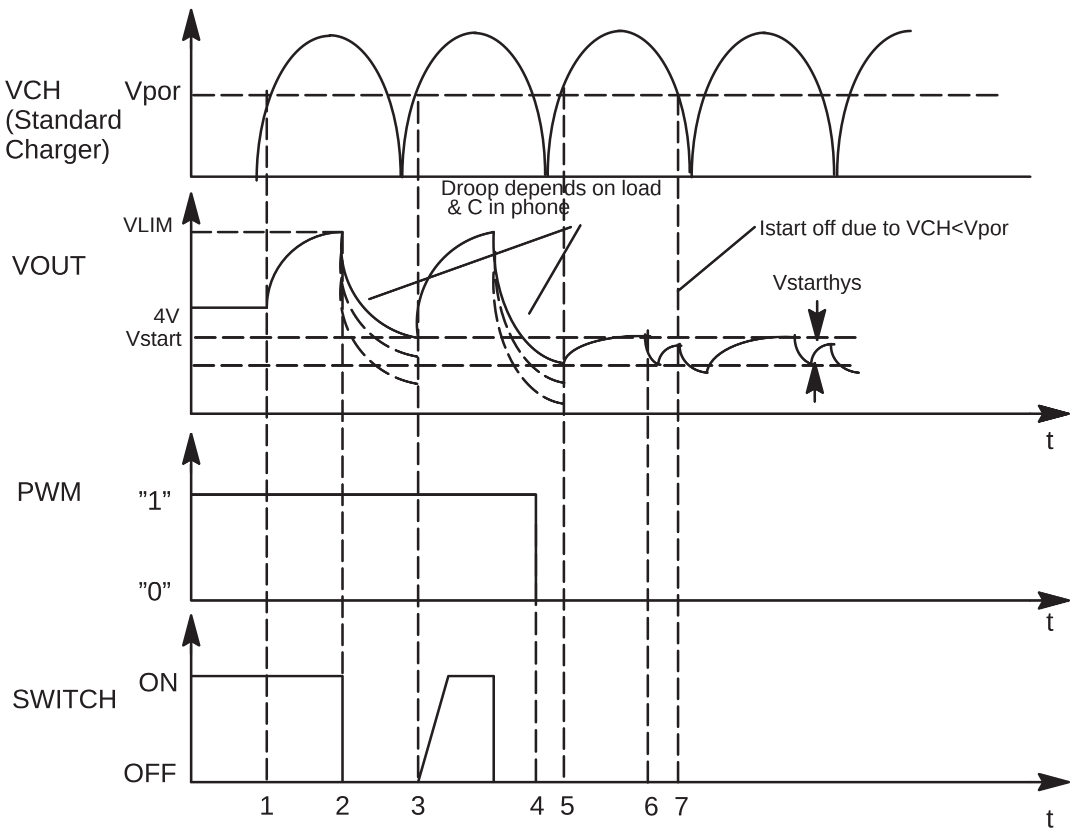
When the switch in output overvoltage situation has once turned OFF, it stays OFF until the the battery voltage falls below VLIM1 (or VLIM2) and PWM = LOW is detected. The switch can be turned on again by setting PWM = HIGH.



Battery Removal During Charging

Output overvoltage protection is also needed in case the main battery is removed when charger connected or charger is connected before the battery is connected to the phone.

With a charger connected, if VOUT exceeds VLIM1 (or VLIM2), CHAPS turns switch OFF until the charger input has sunken below Vpor (nominal 3.0V, maximum 3.4V). MCU software will stop the charging (turn off PWM) when it detects that battery has been removed. The CHAPS remains in protection state as long as PWM stays HIGH after the output overvoltage situation has occured.

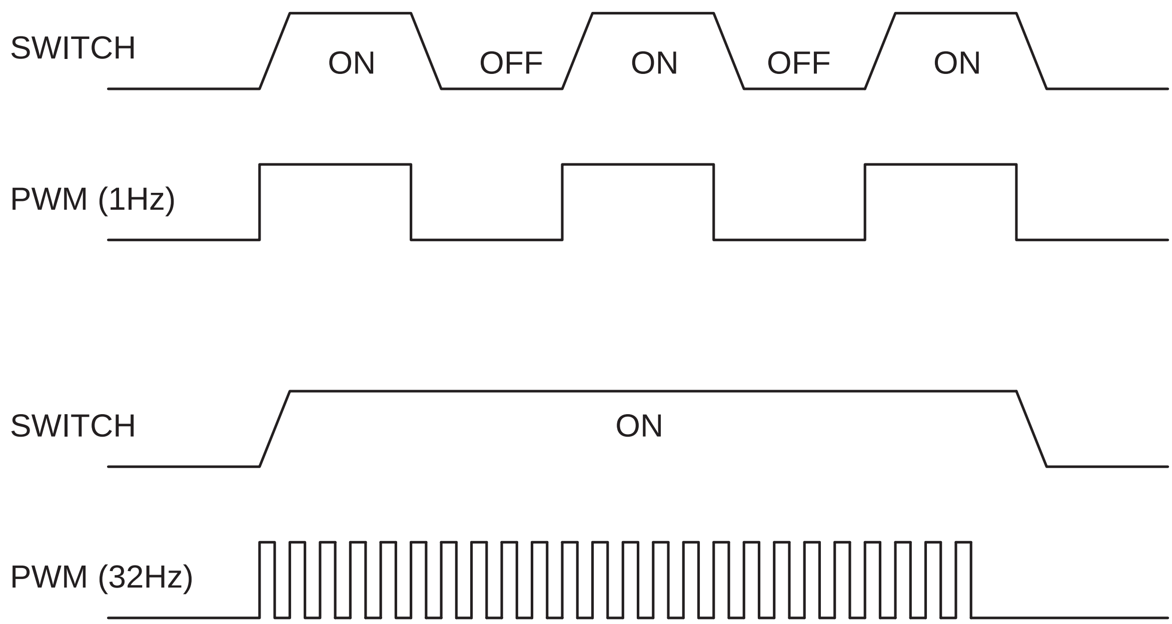


1. Battery removed, (standard) charger connected, VOUT rises (follows charger voltage)
2. VOUT exceeds limit VLIM(X), switch is turned immediately OFF
3. VOUT falls (because no battery) , also VCH<Vpor (standard chargers full–rectified output). When VCH > Vpor and VOUT < VLIM(X) –> switch turned on again (also PWM is still HIGH) and VOUT again exceeds VLIM(X).
4. Software sets PWM = LOW –> CHAPS does not enter PWM mode
5. PWM low –> Startup mode, startup current flows until Vstart limit reached
6. VOUT exceeds limit Vstart, Istart is turned off
7. VCH falls below Vpor

Different PWM Frequencies (1Hz and 32 Hz)

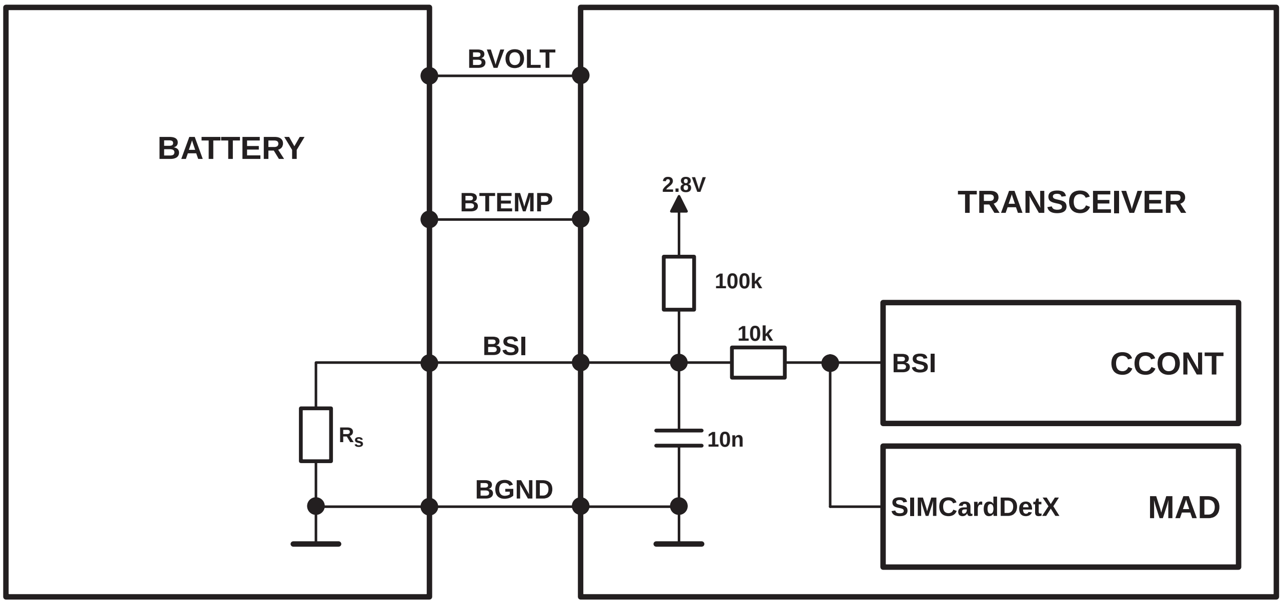
When a travel charger (2– wire charger) is used, the power switch is turned ON and OFF by the PWM input when the PWM rate is 1Hz. When PWM is HIGH, the switch is ON and the output current Iout = charger current – CHAPS supply current. When PWM is LOW, the switch is OFF and the output current Iout = 0. To prevent the switching transients inducing noise in audio circuitry of the phone soft switching is used.

The performance travel charger (3– wire charger) is controlled with PWM at a frequency of 32Hz. When the PWM rate is 32Hz CHAPS keeps the power switch continuously in the ON state.

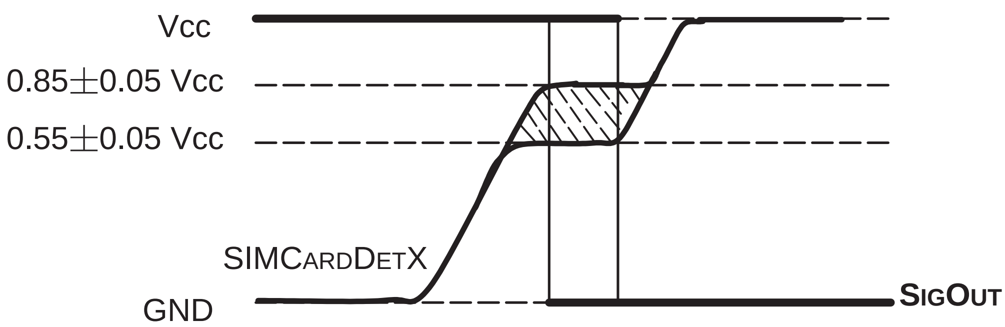


Battery Identification

Different battery types are identified by a pulldown resistor inside the battery pack. The BSI line inside transceiver has a 100k pullup to VBB. The MCU can identify the battery by reading the BSI line DC–voltage level with a CCONT (N100) A/D–converter.

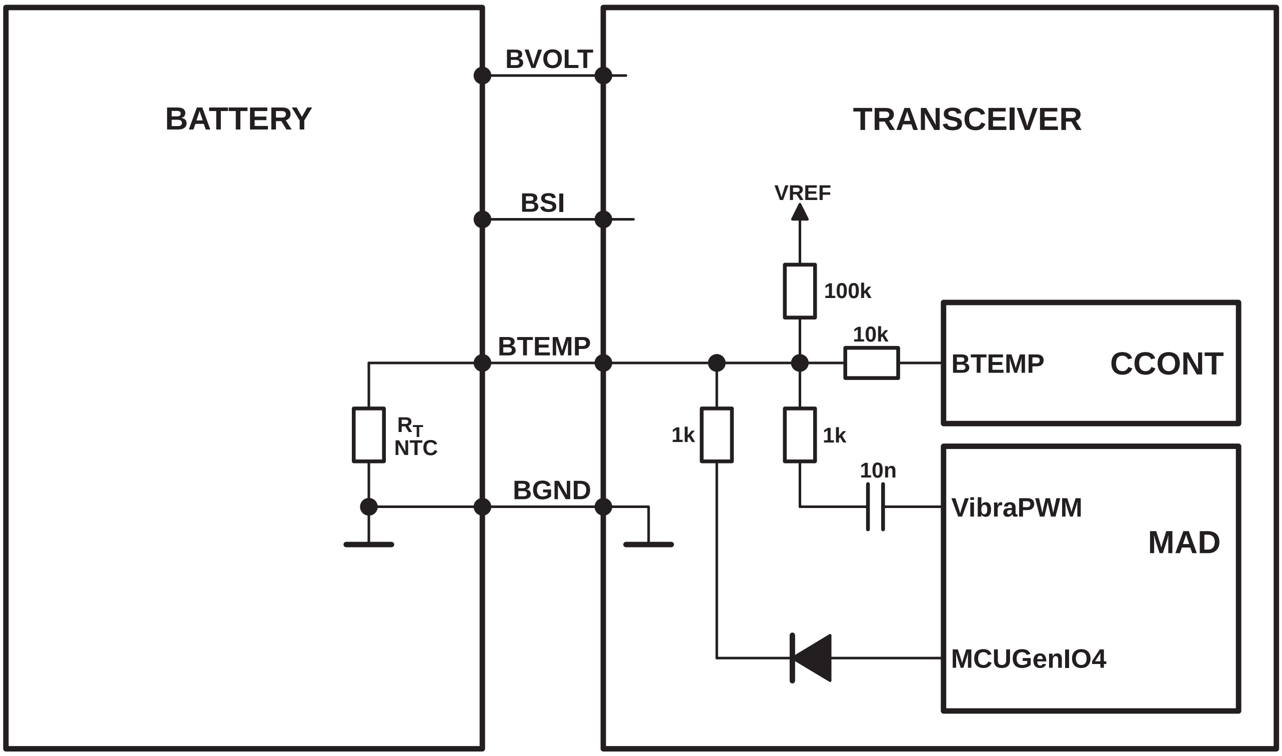


The battery identification line is used also for battery removal detection. The BSI line is connected to a SIMCardDetX line of MAD2 (D200). SIMCardDetX is a threshold detector with a nominal input switching level 0.85xVcc for a rising edge and 0.55xVcc for a falling edge. The battery removal detection is used as a trigger to power down the SIM card before the power is lost. The BSI contact in the battery pack is made 0.7mm shorter than the supply voltage contacts so that there is a delay between battery removal detection and supply power off,



Battery Temperature

The battery temperature is measured with a NTC inside the battery pack. The BTEMP line inside transceiver has a 100k pullup to VREF. The MCU can calculate the battery temperature by reading the BTEMP line DC–voltage level with a CCONT (N100) A/D–converter.



Supply Voltage Regulators

The heart of the power distrubution is the CCONT. It includes all the voltage regulators and feeds the power to the whole system. The baseband digital parts are powered from the VBB regulator which provides 2.8V baseband supply. The baseband regulator is active always when the phone is powered on. The VBB baseband regulator feeds MAD and memories, COBBA digital parts and the LCD driver in the UI section. There is a separate regulator for a SIM card. The regulator is selectable between 3V and 5V and controlled by the SIMPwr line from MAD to CCONT. The COBBA analog parts are powered from a dedicated 2.8V supply VCOBBA. The CCONT supplies also 5V for RF and for flash VPP. The CCONT contains a real time clock function, which is powered from a RTC backup when the main battery is disconnected.

The RTC backup is rechargable polyacene battery, which has a capacity of 50uAh (@3V/2V) The battery is charged from the main battery voltage by the CHAPS when the main battery voltage is over 3.2V. The charging current is 200uA (nominal).

Operating mode	Vref	RF REG	VCOB-BA	VBB	VSIM	SIMIF
Power off	Off	Off	Off	Off	Off	Pull down
Power on	On	On/Off	On	On	On	On/Off
Reset	On	Off VR1 On	On	On	Off	Pull down
Sleep	On	Off	On	On	On	On/Off

NOTE:

CCONT includes also five additional 2.8V regulators providing power to the RF section. These regulators can be controlled either by the direct control signals from MAD or by the RF regulator control register in CCONT which MAD can update. Below are the listed the MAD control lines and the regulators they are controlling.

- TxPwr controls VTX regulator (VR5)
- RxPwr controls VRX regulator (VR2)
- SynthPwr controls VSYN_1 and VSYN_2 regulators (VR4 and VR3)
- VCXOPwr controls VXO regulator (VR1)

CCONT generates also a 1.5 V reference voltage VREF to COBBA, SUMMA and CRFU3. The VREF voltage is also used as a reference to some of the CCONT A/D converters.

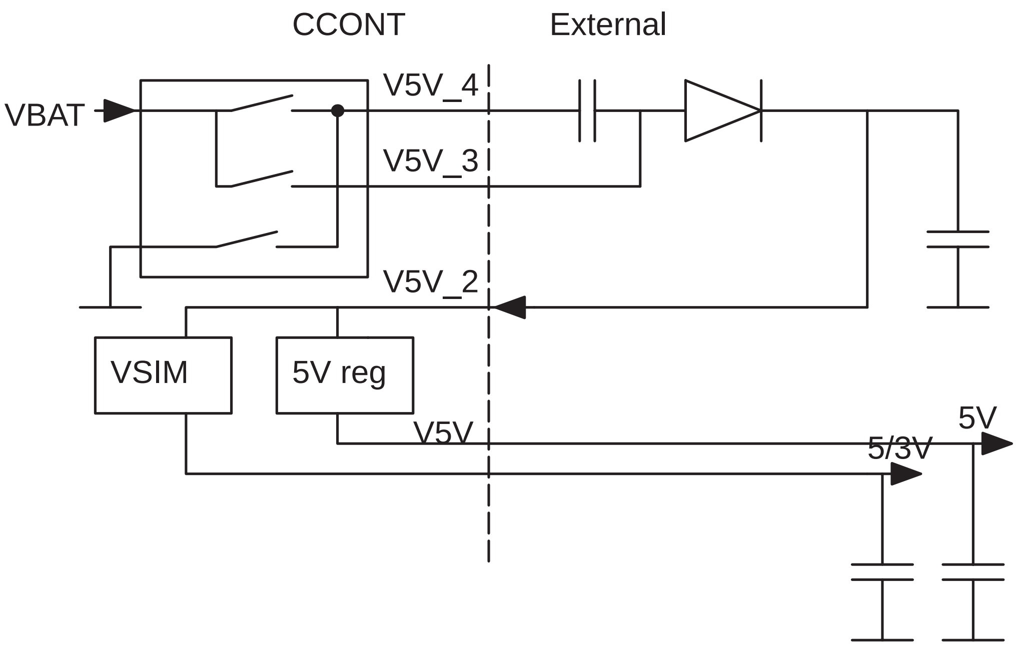
In additon to the above mentioned signals MAD includes also TXP control signal which goes to SUMMA power control block and to the power amplifier. The transmitter power control TXC is led from COBBA to SUMMA.

Switched Mode Supply VSIM

There is a switched mode supply for SIM–interface. SIM voltage is selected via serial IO. The 5V SMR can be switched on independently of the SIM voltage selection, but can't be switched off when VSIM voltage value is set to 5V.

NOTE: VSIM and V5V can give together a total of 30mA.

In the next figure the principle of the SMR / VSIM–functions is shown.



Power Up

The baseband is powered up by:

1. Pressing the power key, that generates a PWRONX interrupt signal from the power key to the CCONT, which starts the power up procedure.
2. Connecting a charger to the phone. The CCONT recognizes the charger from the VCHAR voltage and starts the power up procedure.
3. A RTC interrupt. If the real time clock is set to alarm and the phone is switched off, the RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is connected to the PWRONX line to give a power on signal to the CCONT just like the power key.
4. A battery interrupt. Intelligent battery packs have a possibility to power up the phone. When the battery gives a short (10ms) voltage pulse through the BTEMP pin, the CCONT wakes up and starts the power on procedure.

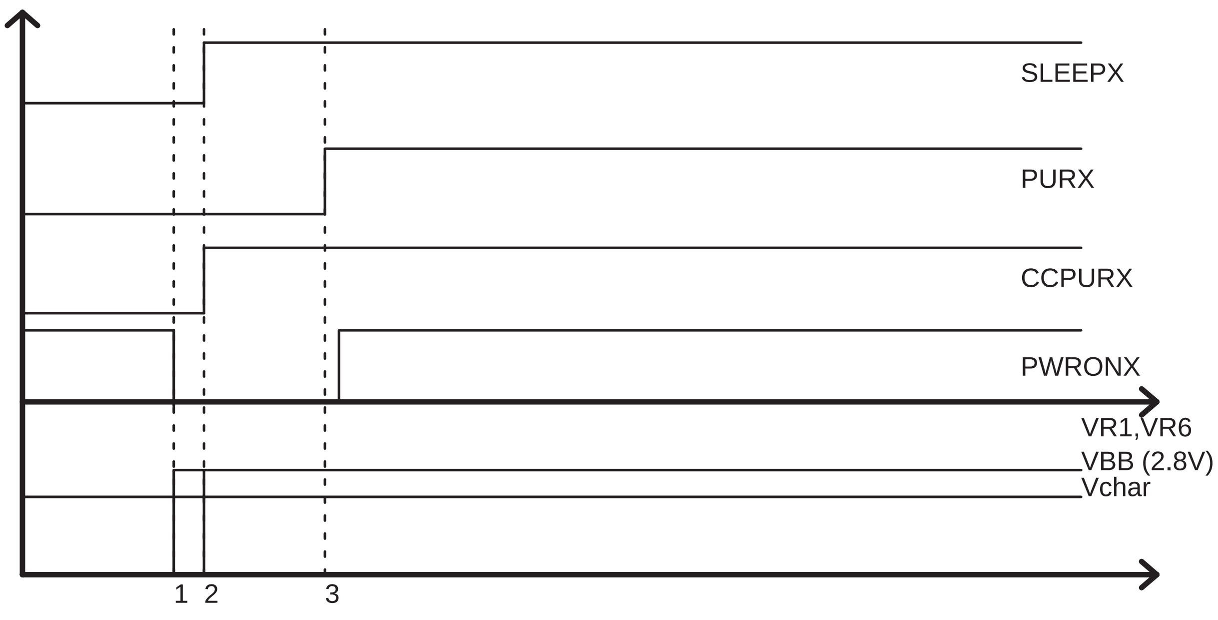
Power up with a charger

When the charger is connected CCONT will switch on the CCONT digital voltage as soon as the battery voltage exeeds 3.0V. The reset for CCONT’s digital parts is released when the operating voltage is stabilized (50 us from switching on the voltages). Operating voltage for VCXO is also switched on. The counter in CCONT digital section will keep MAD in reset for 62 ms (PURX) to make sure that the clock provided by VCXO is stable. After this delay MAD reset is relased, and VCXO –control (SLEEPX) is given to MAD. The diagram assumes empty battery, but the situation would be the same with full battery:

When the phone is powered up with an empty battery pack using the standard charger, the charger may not supply enough current for standard powerup procedure and the powerup must be delayed.

Power Up With The Power Switch (PWRONX)

When the power on switch is pressed the PWRONX signal will go low. CCONT will switch on the CCONT digital section and VCXO as was the case with the charger driven power up. If PWRONX is low when the 64 ms delay expires, PURX is released and SLEEPX control goes to MAD. If PWRONX is not low when 64 ms expires, PURX will not be released, and CCONT will go to power off (digital section will send power off signal to analog parts)



1:Power switch pressed ==> Digital voltages on in CCONT (VBB)
2: CCONT digital reset released. VCXO turned on
3: 62 ms delay to see if power switch is still pressed.

Power Up by RTC

RTC (internal in CCONT) can power the phone up by changing RTCPwr to logical ”1”. RTCPwr is an internal signal from the CCONT digital section.

Power Up by IBI

IBI can power CCONT up by sending a short pulse to logical ”1”. RTCPwr is an internal signal from the CCONT digital section.

Acting Dead

If the phone is off when the charger is connected, the phone is powered on but enters a state called ”acting dead”. To the user the phone acts as if it was switched off. A battery charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active Mode

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. All the CCONT regulators are operating. There are several substates in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc..

Sleep Mode

In the sleep mode, all the regulators except the baseband VBB, VCOBBA, and the SIM card VSIM regulators are off. Sleep mode is activated by the MAD after MCU and DSP clocks have been switched off. The voltage regulators for the RF section are switched off and the VCXO power control, VCXOPwr is set low. In this state only the 32 kHz sleep clock oscillator in CCONT is running. The flash memory power down input is connected to the ExtSysResetX signal, and the flash is deep powered down during the sleep mode.

The sleep mode is exited either by the expiration of a sleep clock counter in the MAD or by some external interrupt, generated by a charger connection, key press, headset connection etc. The MAD starts the wake up sequence and sets the VCXOPwr and ExtSysResetX control high. After VCXO settling time other regulators and clocks are enabled for active mode.

If the battery pack is disconnect during the sleep mode, the CCONT pulls the SIM interface lines low as there is no time to wake up the MCU.

Charging

Charging can be performed in any operating mode. The charging algorithm is dependent on the used battery technology. The battery type is indicated by a resistor inside the battery pack. The resistor value corresponds to a specific battery capacity. This capacity value is related to the battery technology as different capacity values are achieved by using different battery technology.

The battery voltage, temperature, size and current are measured by the CCONT controlled by the charging software running in the MAD.

The power management circuitry controls the charging current delivered from the charger to the battery. Charging is controlled with a PWM input signal, generated by the CCONT. The PWM pulse width is controlled by the MAD and sent to the CCONT through a serial data bus. The battery voltage rise is limited by turning the CHAPS switch off when the battery voltage has reached 4.2V (LiIon) or 5.2V (NiMH, 5V in call mode). Charging current is monitored by measuring the voltage drop across a 220mohm resistor.

Power Off

The baseband is powered down by:

1. Pressing the power key, that is monitored by the MAD, which starts the power down procedure.
2. If the battery voltage is dropped below the operation limit, either by not charging it or by removing the battery.
3. Letting the CCONT watchdog expire, which switches off all CCONT regulators and the phone is powered down.
4. Setting the real time clock to power off the phone by a timer. The RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is connected to the PWRONX line to give a power off signal to the CCONT just like the power key.

The power down is controlled by the MAD. When the power key has been pressed long enough or the battery voltage is dropped below the limit the MCU initiates a power down procedure and disconnects the SIM power. Then the MCU outputs a system reset signal and resets the DSP. If there is no charger connected the MCU writes a short delay to CCONT watchdog and resets itself. After the set delay the CCONT watchdog expires, which activates the PURX and all regulators are switched off and the phone is powered down by the CCONT.

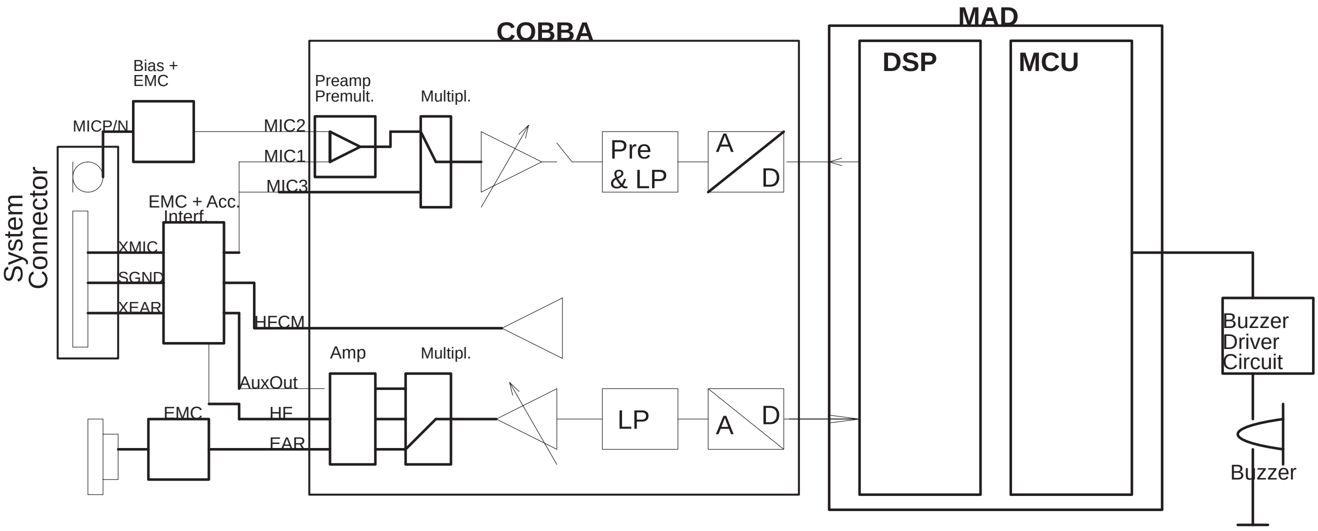
If a charger is connected when the power key is pressed the phone enters into the acting dead mode.

Watchdog

The Watchdog block inside CCONT contains a watchdog counter and some additional logic which are used for controlling the power on and power off procedures of CCONT. Watchdog output is disabled when WDDisX pin is tied low. The WD-counter runs during that time, though. Watchdog counter is reset internally to 32s at power up. Normally it is reset by MAD writing a control word to the WDReg.

Audio control

The audio control and processing is taken care by the COBBA–GJ, which contains the audio and RF codecs, and the MAD2, which contains the MCU, ASIC and DSP blocks handling and processing the audio signals. A detailed audio specification can be found from document



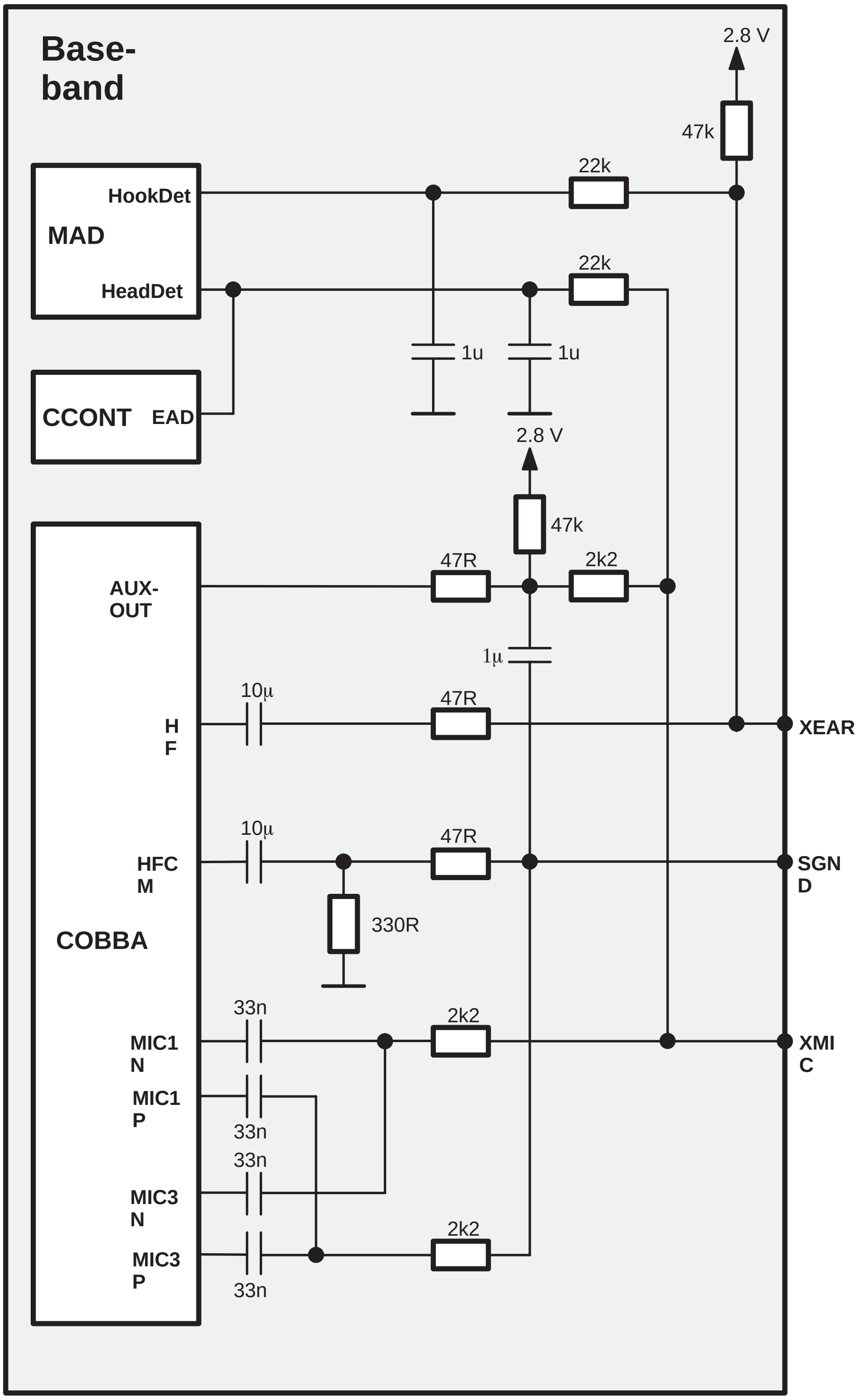
The baseband supports three microphone inputs and two earphone outputs. The inputs can be taken from an internal microphone, a headset microphone or from an external microphone signal source. The microphone signals from different sources are connected to separate inputs at the COBBA–GJ asic. Inputs for the microphone signals are differential type.

The MIC1 inputs are used for a headset microphone that can be connected directly to the system connector. The internal microphone is connected to MIC2 inputs and an external pre–amplified microphone (handset/handfree) signal is connected to the MIC3 inputs. In COBBA there are also three audio signal outputs of which dual ended EAR lines are used for internal earpiece and HF line for accessory audio output. The third audio output AUXOUT is used only for bias supply to the headset microphone. As a difference to DCT2 generation the SGND (= HFCM at COBBA) does not supply audio signal (only common mode). Therefore there are no electrical loopback echo from downlink to uplink.

The output for the internal earphone is a dual ended type output capable of driving a dynamic type speaker. The output for the external accessory and the headset is single ended with a dedicated signal ground SGND. Input and output signal source selection and gain control is performed inside the COBBA–GJ asic according to control messages from the MAD2. Keypad tones, DTMF, and other audio tones are generated and encoded by the MAD2 and transmitted to the COBBA–GJ for decoding.

External Audio Connections

The external audio connections are presented in figure 16. A headset can be connected directly to the system connector. The headset microphone bias is supplied from COBBA AUXOUT output and fed to microphone through XMIC line. The 330ohm resistor from SGND line to AGND provides a return path for the bias current.



Analog Audio Accessory Detection

In XEAR signal there is a 47 kΩ pullup in the transceiver and 6.8 kΩ pull–down to SGND in accessory. The XEAR is pulled down when an accessory is connected, and pulled up when disconnected. The XEAR is connected to the HookDet line (in MAD), an interrupt is given due to both connection and disconnection. There is filtering between XEAR and HookDet to prevent audio signal giving unwanted interrupts.

External accessory notices powered–up phone by detecting voltage in XMIC line. In Table 23 there is a truth table for detection signals.

Accessory connected	HookDet	HeadDet	Notes
No accessory connected	High	High	Pullups in the transceiver
Headset HDC–9 with a button switch pressed	Low	Low	XEAR and XMIC loaded (dc)
Headset HDC–9 with a button switch released	High	Low *)	XEAR unloaded (dc)
Handsfree (HFU–1)	Low	High	XEAR loaded (dc)

Headset Detection

The external headset device is connected to the system connector, from which the signals are routed to COBBA headset microphone inputs and earphone outputs. In the XMIC line there is a (47 + 2.2) kΩ pullup in the transceiver. The microphone is a low resistance pulldown compared to the transceiver pullup.

When there is no call going, the AUXOUT is in high impedance state and the XMIC is pulled up. When a headset is connected, the XMIC is pulled down. The XMIC is connected to the HeadDet line (in MAD), an interrupt is given due to both connection and disconnection. There is filtering between the XMIC and the HeadDet to prevent audio signal giving unwanted interrupts (when an accessory is connected).

In the XEAR line there is a 47 kΩ pullup in the transceiver. The earphone is a low resistance pulldown compared to the transceiver pullup. When a remote control switch is open, there is a capacitor in series with the earphone, so the XEAR (and HookDet) is pulled up by the phone. When the switch is closed, the XEAR (and HookDet) is pulled down via the earphone. So both press and release of the button gives an interrupt.

During a call there is a bias voltage (1.5 V) in the AUXOUT, and the HeadDet cannot be used. The headset interrupts should to be disabled during a call and the EAD line (AD converter in CCONT) should be polled to see if the headset is disconnected.

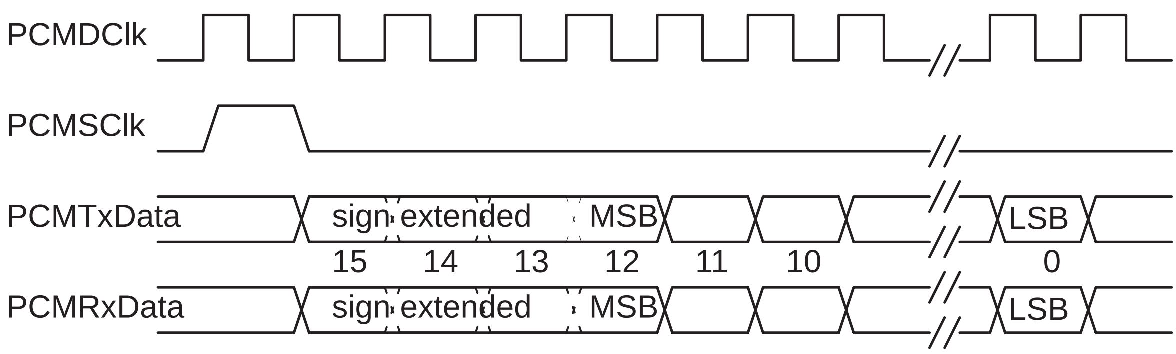
Internal Audio Connections

The speech coding functions are performed by the DSP in the MAD2 and the coded speech blocks are transferred to the COBBA–GJ for digital to analog conversion, down link direction. In the up link direction the PCM coded speech blocks are read from the COBBA–GJ by the DSP.

There are two separate interfaces between MAD2 and COBBA–GJ: a parallel bus and a serial bus. The parallel bus has 12 data bits, 4 address bits, read and write strobes and a data available strobe. The parallel interface is used to transfer all the COBBA–GJ control information (both the RFI part and the audio part) and the transmit and receive samples. The serial interface between MAD2 and COBBA–GJ includes transmit and receive data, clock and frame synchronisation signals. It is used to transfer the PCM samples. The frame synchronisation frequency is 8 kHz which indicates the rate of the PCM samples and the clock frequency is 1 MHz. COBBA is generating both clocks.

4–wire PCM Serial Interface

The interface consists of following signals: a PCM codec master clock (PCMDClk), a frame synchronization signal to DSP (PCMSClk), a codec transmit data line (PCMTX) and a codec receive data line (PCMRX). The COBBA–GJ generates the PCMDClk clock, which is supplied to DSP SIO. The COBBA–GJ also generates the PCMSClk signal to DSP by dividing the PCMDClk. The PCMDClk frequency is 1.000 MHz and is generated by dividing the RFIClk 13 MHz by 13. The COBBA–GJ further divides the PCMDClk by 125 to get a PCMSClk signal, 8.0 kHz.



Alert Signal Generation

A buzzer is used for giving alerting tones and/or melodies as a signal of an incoming call. Also keypress and user function response beeps are generated with the buzzer. The buzzer is controlled with a BuzzerPWM output signal from the MAD. A dynamic type of buzzer must be used since the supply voltage available can not produce the required sound pressure for a piezo type buzzer. The low impedance buzzer is connected to an output transistor that gets drive current from the PWM output. The alert volume can be adjusted either by changing the pulse width causing the level to change or by changing the frequency to utilize the resonance frequency range of the buzzer.

A vibra alerting device is used for giving silent signal to the user of an incoming call. The device is controlled with a VibraPWM output signal from the MAD2. The vibra alert can be adjusted either by changing the pulse width or by changing the pulse frequency. The vibra device is not inside the phone, but in a special vibra battery.

Digital Control

The baseband functions are controlled by the MAD asic, which consists of a MCU, a system ASIC and a DSP.

MAD2

MAD2 contains following building blocks:

- ARM RISC processor with both 16–bit instruction set (THUMB mode) and 32–bit instruction set (ARM mode)
- TI Lead DSP core with peripherials:
    - API (Arm Port Interface memory) for MCU–DSP communication, DSP code download, MCU interrupt handling vectors (in DSP RAM) and DSP booting
    - Serial port (connection to PCM)
    - Timer
    - DSP memory
- BUSC (BusController for controlling accesses from ARM to API, System Logic and MCU external memories, both 8– and 16–bit memories)
- System Logic
    - CTSI (Clock, Timing, Sleep and Interrupt control)
    - MCUIF (Interface to ARM via BusC). Contains MCU BootROM
    - DSPIF (Interface to DSP)
    - MFI (Interface to COBBA AD/DA Converters)

– CODER (Block encoding/decoding and A51&A52 ciphering)
– AccIF(Accessory Interface)
– SCU (Synthesizer Control Unit for controlling 2 separate synthesizer)
– UIF (Keyboard interface, serial control interface for COBBA PCM Codec, LCD Driver and CCONT)
– SIMI (SimCard interface with enhanced features)
– PUP (Parallel IO, USART and PWM control unit for vibra and buzzer)

The MAD2 operates from a 13 MHz system clock, which is generated from the 13Mhz VCXO frequency. The MAD2 supplies a 6,5MHz or a 13MHz internal clock for the MCU and system logic blocks and a 13MHz clock for the DSP, where it is multiplied to 52 MHz DSP clock. The system clock can be stopped for a system sleep mode by disabling the VCXO supply power from the CCONT regulator output. The CCONT provides a 32kHz sleep clock for internal use and to the MAD2, which is used for the sleep mode timing. The sleep clock is active when there is a battery voltage available i.e. always when the battery is connected.

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
1	MCUGenOut5	O	Audio	2	0		MCU General purpose output port
2	MCUGenOut4	O	N101	2	0		MCU General purpose output port
3	*LEADGND*						Lead Ground
4	MCUGenOut3	O		2	0		MCU General purpose output port
5	**VCC**					IO VCC in 3325c10	Power
6	MCUGenOut2	O		2	0		MCU General purpose output port
7	MCUGenOut1	O	MCU memory	2	0		MCU General purpose output port
8	MCUGenOut0	O		2	1	LoByteSelX in 16–bit mode	MCU General purpose output port
9	Col4	I/O	UIF	2	Input	programmable pullup PR0201	I/O line for keyboard column 4

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
10	Col3	I/O	UIF	2	Input	program-mable pullup PR0201	I/O line for key-board column 3
11	**GND**						Ground
12	Col2	I/O	UIF	2	Input	program-mable pullup PR0201	I/O line for key-board column 2
13	Col1	I/O	UIF	2	Input	program-mable pullup PR0201	I/O line for key-board column 1
14	Col0	I/O	UIF	2	Input	program-mable pullup PR0201	I/O line for key-board column 0
15	LCDCSX	I/O	UIF	2	Input	external pullup/down	serial LCD driver chip select, par-allel LCD driver enable
16	*LEADVCC*						Lead Power
17	Row5LCDCD	I/O	UIF	2	Input, pullup	pullup PR0201	Keyboard row5 data I/O , serial LCD driver com-mand/data indi-cator, parallel LCD driver read/ write select
18	**VCC**					Core VCC in 3325c10	Power
19	Row4	I/O	UIF	2	Input, pullup	pullup PR0201	I/O line for key-board row 4, par-allel LCD driver register selection control
20	Row3	I/O	UIF	2	Input, pullup	pullup PR0201	I/O line for key-board row 3, par-allel LCD driver data
21	Row2	I/O	UIF	2	Input, pullup	pullup PR0201	I/O line for key-board row 2, par-allel LCD driver data
22	Row1	I/O	UIF	2	Input, pullup	pullup PR0201	I/O line for key-board row 1, par-allel LCD driver data
23	Row0	I/O	UIF	2	Input, pullup	pullup PR0201	I/O line for key-board row 0, par-allel LCD driver data

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
24	JTDO	O		2	Tri–state		JTAG data out
25	**GND**						Ground
26	JTRst	I			Input, pull-down	pulldown PD0201	JTAG reset
27	JTClk	I			Input	pulldown PD0201	JTAG Clock
28	JTDI	I			Input, pullup	pullup PR0201	JTAG data in
29	JTMS	I			Input, pullup	pullup PR0201	JTAG mode se-lect
30	**VCC**					IO VCC in 3325c10	Power
31	CoEmu0	I/O		2	Input, pullup	pullup PR0201	DSP/MCU emulation port 0
32	CoEmu1	I/O		2	Input, pullup	pullup PR0201	DSP/MCU emulation port 1
33	MCUGenIO7	I/O		2	Input, pull-down	pulldown PD1001	General purpose I/O port
34	MCUGenIO6	I/O	UI	2	Input, pull-down	pulldown PD1001	Lights
35	*LEADGND*						Lead Ground
36	MCUGenIO5	I/O	UI	2	Input, pull-down	pulldown PD1001	LCD reset
37	*ARMGND*						ARM Ground
38	MCUAd0	O	MCU MEMORY	2	0		MCU address bus
39	*ARMVCC*						ARM Power
40	MCUAd1	O	MCU MEMORY	2	0		MCU address bus
41	MCUAd2	O	MCU MEMORY	2	0		MCU address bus
42	**GND**						Ground
43	MCUAd3	O	MCU MEMORY	2	0		MCU address bus
44	MCUAd4	O	MCU MEMORY	2	0		MCU address bus
45	MCUAd5	O	MCU MEMORY	2	0		MCU address bus

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
46	MCUAd6	O	MCU MEMORY	2	0		MCU address bus
47	**VCC**					IO VCC in 3325c10	Power
48	MCUAd7	O	MCU MEMORY	2	0		MCU address bus
49	MCUAd8	O	MCU MEMORY	2	0		MCU address bus
50	MCUAd9	O	MCU MEMORY	2	0		MCU address bus
51	MCUAd10	O	MCU MEMORY	2	0		MCU address bus
52	**GND**						Ground
53	MCUAd11	O	MCU MEMORY	2	0		MCU address bus
54	MCUAd12	O	MCU MEMORY	2	0		MCU address bus
55	MCUAd13	O	MCU MEMORY	2	0		MCU address bus
56	MCUAd14	O	MCU MEMORY	2	0		MCU address bus
57	MCUAd15	O	MCU MEMORY	2	0		MCU address bus
58	MCUAd16	O	MCU MEMORY	2	0		MCU address bus
59	**VCC**					Core VCC in 3325c10	Power
60	MCUAd17	O	MCU MEMORY	2	0		MCU address bus
61	MCUAd18	O	MCU MEMORY	2	0		MCU address bus
62	MCUAd19	O	MCU MEMORY	2	0		MCU address bus
63	MCUAd20	O	MCU MEMORY	2	0		MCU address bus
64	MCUAd21	O	MCU MEMORY	2	0		MCU address bus
65	ExtMCUDa0	I/O	MCU MEMORY	2	Input		MCU data bus
66	**GND**						Ground
67	ExtMCUDa1	I/O	MCU MEMORY	2	Output		MCU data bus
68	ExtMCUDa2	I/O	MCU MEMORY	2	Output		MCU data bus

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
69	ExtMCUDa3	I/O	MCU MEMORY	2	Output		MCU data bus
70	ExtMCUDa4	I/O	MCU MEMORY	2	Output		MCU data bus
71	ExtMCUDa5	I/O	MCU MEMORY	2	Output		MCU data bus
72	ExtMCUDa6	I/O	MCU MEMORY	2	Output		MCU data bus
73	**VCC**					IO VCC in 3325c10	Power
74	ExtMCUDa7	I/O	MCU MEMORY	2	Output		MCU data bus
75	MCUGenIO8	I/O		2	Input	MCU Data in 16–bit mode	General purpose I/O port
76	MCUGenIO9	I/O		2	Input	MCU Data in 16–bit mode	General purpose I/O port
77	MCUGenIO10	I/O		2	Input	MCU Data in 16–bit mode	General purpose I/O port
78	MCUGenIO11	I/O		2	Input	MCU Data in 16–bit mode	General purpose I/O port
79	**GND**						Ground
80	MCUGenIO12	I/O		2	Input	MCU Data in 16–bit mode	General purpose I/O port
81	MCUGenIO13	I/O		2	Input	MCU Data in 16–bit mode	General purpose I/O port
82	MCUGenIO14	I/O		2	Input	MCU Data in 16–bit mode	General purpose I/O port
83	MCUGenIO15	I/O		2	Input	MCU Data in 16–bit mode	General purpose I/O port
84	MCURdX	O	MCU MEMORY	2	1		MCU Read strobe
85	**VCC**					Core VCC in 3325c10	Power
86	MCUWrX	O	MCU MEMORY	2	1		MCU write strobe
87	ROM1SelX	O	MCU ROM	2	1		ROM chip select
88	RAMSelX	O	MCU RAM	2	1		RAM chip select
89	ROM2SelX	O	MCU ROM2	2	1		Extra chip select, can be used as MCU general output
90	MCUGenIO1	I/O		2	Input, pullup	pullup PR0201	General purpose I/O port
91	DSPXF	O		2	1		External flag

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
92	*SCVCC*						Special cell Power
93	RFClk	I	VCXO		Input		System clock from VCTCXO
94	RFClkGnd				Input		System clock reference ground input
95	SIMCardDetX	I			Input		SIM card detection
96	*SCGND*						Special cell Ground
97	BuzzPWM	O	BUZZER	2	0		Buzzer PWM control
98	*LEADVCC*						LEAD Power
99	VibraPWM	O	VIBRA	2	0		Vibra PWM control
100	**GND**						Ground
101	MCUGenIO3	I/O	EEPROM	2	Input, pullup	pullup PR1001	General purpose I/O port
102	MCUGenIO2	I/O	EEPROM	2	Input, pullup	pullup PR1001	WP SCL
103	EEPROMSelX	O	MCU EEPROM	2	1		EEPROM chip select, can be used as MCU general output
104	AccTxData	I/O		4	Tri–State	external pullup	Accessory TX data, Flash_TX
105	**VCC**					IO VCC in 3325c10	Power
106	GenDet	I			Input		General purpose interrupt
107	HookDet	I			Input		Non–MBUS accessory connection detector
108	HeadDet	I			Input		Headset detection interrupt
109	AccRxData	I			Input		Accessory RX data, Flash_RX
110	**GND**						Ground
111	MCUGenIO4	I/O		2	Input, pulldown	pulldown PD1001	General purpose I/O port

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
112	MBUS	I/O		2	Input, exter-nal pullup	external pullup	MBUS, Flash clock
113	VCXOPwr	O	CCONT	2	1		VCXO regulator control
114	SynthPwr	O	CCONT	2	0		Synthesizer reg-ulator control
115	**VCC**					Core VCC in 3325c10	Power
116	GenCCONTCSX	O	CCONT	2	1		Chip select to CCONT
117	*LEADGND*						LEAD Ground
118	GenSDIO	I/O	CCONT, UIF	2	Input, exter-nal pullup/ down	external pullup/down depending on how to boot	Serial data in/out
119	GenSClk	O	CCONT, UIF	2	0		Serial clock
120	SIMCardData	I/O	CCONT	2	0		SIM data
121	**GND**						Ground
122	PURX	I	CCONT		Input		Power Up Reset
123	CCONTInt	I	CCONT		Input		CCONT interrupt
124	Clk32k	I	CCONT		Input		Sleep clock os-cillator input
125	**VCC**					IO VCC in 3325c10	Power
126	SIMCardClk	O	CCONT	2	0		SIM clock
127	SIMCardRstX	O	CCONT	2	0		SIM reset
128	SIMCardIOC	O	CCONT	2	0		SIM data in/out control
129	SIMCardPwr	O	CCONT	2	0		SIM power con-trol
130	*LEADVCC*						LEAD Power
131	RxPwr	O	CCONT	2	0		RX regulator control
132	TxPwr	O	CCONT	2	0		TX regulator control
133	TestMode	I			Input, pull-down	pulldown PD0201	Test mode select
134	ExtSysResetX	O		2	0		System Reset

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
135	PCMTxData	O	COBBA	2	0		Transmit data, DX
136	**VCC**					IO VCC in 3325c10	Power
137	PCMRxData	I	COBBA		Input		Receive data, RX
138	PCMDClk	I	COBBA		Input		Transmit clock, CLKX
139	PCMSClk	I	COBBA		Input		Transmitframe sync, FSX
140	COBBADAX	I	COBBA		Input		Data available acknowledge
141	**GND**						Ground
142	COBBAWrX	O	COBBA	2	1		COBBA write strobe
143	COBBARdX	O	COBBA	2	1		COBBA read strobe
144	COBBAClk	O	COBBA	4	1		COBBA clock, 13 MHz
145	COBBAAd3	O	COBBA	2	0		COBBA address bit
146	COBBAAd2	O	COBBA	2	0		COBBA address bit
147	COBBAAd1	O	COBBA	2	0		COBBA address bit
148	COBBAAd0	O	COBBA	2	0		COBBA address bit
149	COBBADa11	I/O	COBBA	2	0		COBBA data bit
150	**VCC**					Core VCC in 3325c10	Power
151	COBBADa10	I/O	COBBA	2	0		COBBA data bit
152	COBBADa9	I/O	COBBA	2	0		COBBA data bit
153	COBBADa8	I/O	COBBA	2	0		COBBA data bit
154	COBBADa7	I/O	COBBA	2	0		COBBA data bit
155	COBBADa6	I/O	COBBA	2	0		COBBA data bit
156	**GND**						Ground
157	COBBADa5	I/O	COBBA	2	0		COBBA data bit
158	COBBADa4	I/O	COBBA	2	0		COBBA data bit
159	COBBADa3	I/O	COBBA	2	0		COBBA data bit
160	COBBADa2	I/O	COBBA	2	0		COBBA data bit
161	COBBADa1	I/O	COBBA	2	0		COBBA data bit

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
162	COBBADa0	I/O	COBBA	2	0		COBBA data bit
163	DSPGenOut5	O	RF	2	0		DSP general purpose output, COBBA reset
164	**VCC**					IO VCC in 3325c10	Power
165	DSPGenOut4	O	CRFU3	2	0		DSP general purpose output, BANDSEL signal
166	DSPGenOut3	O	IR	2	0		IR ON
167	DSPGenOut2	O		2	0		DSP general purpose output
168	DSPGenOut1	O		2	0		DSP general purpose output
169	DSPGenOut0	O		2	0		DSP general purpose output
170	MCUGenIO0	I/O	EEPROM	2	Input, pullup	pullup PR0201	SDA
171	FrACtrl	O	RF	2	0		SDATX0
172	**GND**						Ground
173	SynthEna	O	SUMMA	2	0		Synthesizer data enable
174	SynthClk	O	SUMMA	2	0		Synthesizer clock
175	SynthData	O	SUMMA	2	0		Synthesizer data
176	TxPA	O	SUMMA, power amplifier	2	0		Power amplifier control

Memories

The MCU program code resides in an external flash program memory, which size is 16 Mbits (1024kx16bit). The MCU work (data) memory size is 1 Mbits (128kx8bit). A serial EEPROM is used for storing the system and tuning parameters, user settings and selections, a scratch pad and a short code memory. The EEPROM size is 128kbits (16kx8bit).

The BusController (BUSC) section in the MAD decodes the chip select signals for the external memory devices and the system logic. BUSC controls internal and external bus drivers and multiplexers connected to the MCU data bus. The MCU address space is divided into access areas with separate chip select signals. BUSC supports a programmable number of wait states for each memory range.

Program Memory

The MCU program code resides in the program memory. The program memory size is 16 Mbits (1024kx16bit).

The flash memory has a power down pin that should be kept low, during the power up phase of the flash to ensure that the device is powered up in the correct state, read only. The power down pin is utilized in the system sleep mode by connecting the ExtSysResetX to the flash power down pin to minimize the flash power consumption during the sleep.

SRAM Memory

The work memory is a static ram of size 1Mbit (128kx8) in a shrink TSOP32 package. The work memory is supplied from the common baseband VBB voltage and the memory contents are lost when the baseband voltage is switched off. All retainable data should be stored into the EEPROM (or flash) when the phone is powered down.

EEPROM Memory

An EEPROM is used for a nonvolatile data memory to store the tuning parameters and phone setup information. The short code memory for storing user defined information is also implemented in the EEPROM. The EEPROM size is 128kbits. The memory is accessed through a serial bus and the default package is SO8.

MCU Memory Map

MAD2 supports maximum of 4GB internal and 4MB external address space. External memories use address lines MCUAd0 to MCUAd21 and 16–bit databus. The BUSC bus controller supports 8– and 16–bit access for byte, double byte, word and double word data. Access wait state 2 and used databus width can be selected separately for each memory block.

Flash Programming

The phone have to be connected to the flash loading adapter FLA–5 so that supply voltage for the phone and data transmission lines can be supplied from/to FLA–5. When FLA–5 switches supply voltage to the phone, the program execution starts from the BOOT ROM and the MCU investigates in the early start–up sequence if the flash prommer is connected. This is done by checking the status of the MBUS–line. Normally this line is high but when the flash prommer is connected the line is forced low by the prommer.

The flash prommer serial data receive line is in receive mode waiting for an acknowledgement from the phone. The data transmit line from the baseband to the prommer is initially high. When the baseband has recognized the flash prommer, the TX–line is pulled low. This acknowledgement is used to start to toggle MBUS (FCLK) line three times in order that MAD2 gets initialized. This must be happened within 15 ms after TX line is pulled low. After that the data transfer of the first two bytes from the flash prommer to the baseband on the RX–line must be done within 1 ms.

When MAD2 has received the secondary boot byte count information, it forces TX line high. Now, the secondary boot code must be sent to the phone within 10 ms per 16 bit word. If these timeout values are exceeded, the MCU (MAD2) starts normal code execution from flash. After this, the timing between the phone and the flash prommer is handled with dummy bites.

A 3V programming voltage is supplied inside the transceiver from the battery voltage with a switch mode regulator (3V/30mA) of the CCONT. The 3V is connected to VPP pin of the flash through the UI board.

COBBA–GJ

The COBBA–GJ provides an interface between the baseband and the RF–circuitry. COBBA–GJ performs analogue to digital conversion of the receive signal. For transmit path COBBA_GJ performs digital to analogue conversion of the transmit amplifier power control ramp and the in–phase and quadrature signals. A slow speed digital to analogue converter will provide automatic frequency control (AFC).

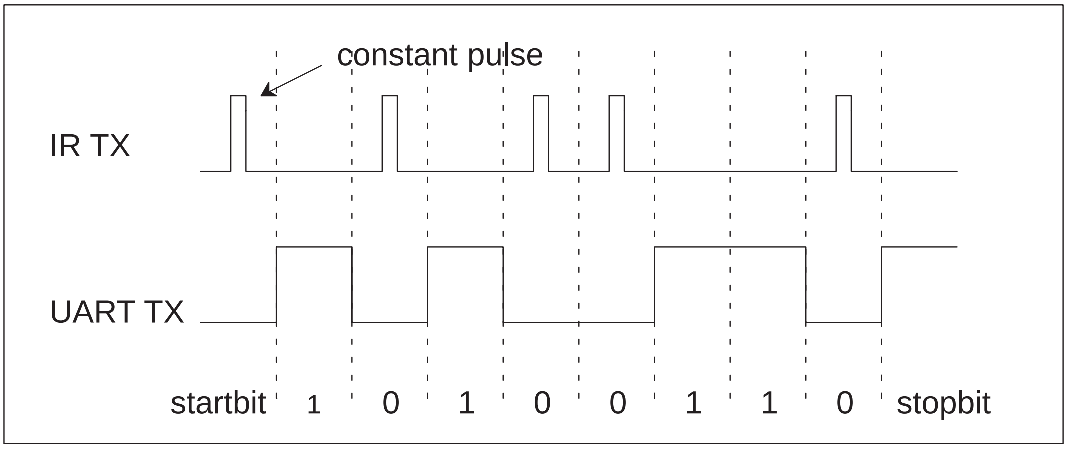
The COBBA asic is at any time connected to MAD asic with two interfaces, one for transferring tx and rx data between MAD and COBBA and one for transferring codec rx/tx samples.

Infrared Transceiver Module

The module is activated with an IRON signal by the MAD, which supplies power to the module. The IR datalines are connected to the MAD accessory interface AccIf via FBUS. The RX and TX lines are separated from FBUS by three–state buffers, when the IR–module is switched off. The AccIf in MAD performs pulse encoding and shaping for transmitted data and detection and decoding for received data pulses.

The data is transferred over the IR link using serial data at speeds 9.6, 19.2, 38.4, 57.6 or 115.2 kbits/s, which leads to maximum throughput of 92.160 kbits/s. The used IR module complies with the IrDA 1.0 specification (Infra Red Data Association), which is based on the HP SIR (Hewlett–Packard's Serial Infra Red) consept.

Following figure gives an example of IR transmission pulses. In IR transmission a light pulse correspondes to 0–bit and a ”dark pulse” correspondes to 1–bit.



The FBUS cannot be used for external accessory communication when the infrared mode is selected, as IR communication reserves the FBUS completely.

Real Time Clock

Requirements for a real time clock implementation are a basic clock (hours and minutes), a calender and a timer with alarm and power on/off –function and miscellaneous calls. The RTC will contain only the time base and the alarm timer but all other functions (e.g. calendar) will be implemented with the MCU software. The RTC needs a power backup to keep the clock running when the phone battery is disconnected. The backup power is supplied from a rechargable polyacene battery that can keep the clock running some ten minutes. If the backup has expired, the RTC clock restarts after the main battery is connected. The CCONT keeps MCU in reset until the 32kHz source is settled (1s max).

The CCONT is an ideal place for an integrated real time clock as the asic already contains the power up/down functions and a sleep control with the 32kHz sleep clock, which is running always when the phone battery is connected. This sleep clock is used for a time source to a RTC block.

RTC backup battery charging

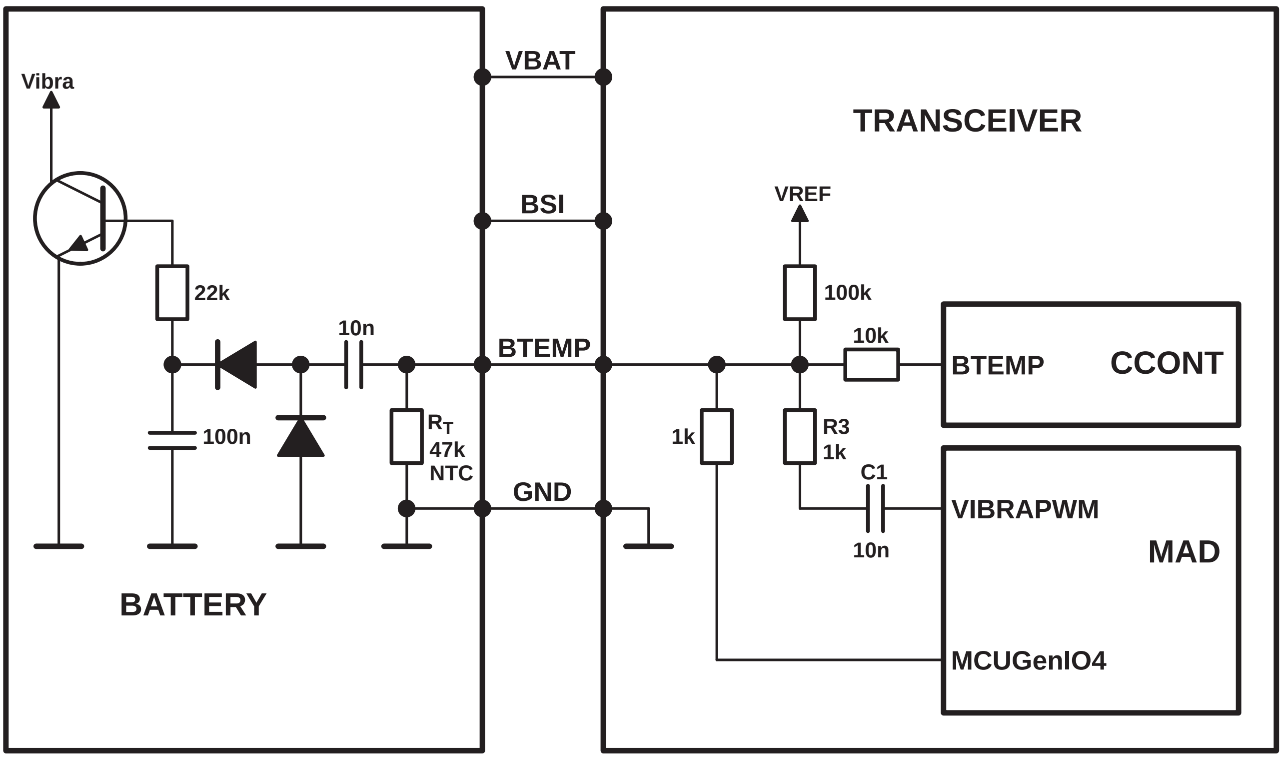
CHAPS has a current limited voltage regulator for charging a backup battery. The regulator derives its power from VOUT so that charging can take place without the need to connect a charger. The backup battery is only used to provide power to a real time clock when VOUT is not present so it is important that power to the charging circuitry is derived from VOUT and that the charging circuitry does not present a load to the backup battery when VOUT is not present.

It should not be possible for charging current to flow from the backup battery into VOUT if VOUT happens to be lower than VBACK. Charging current will gradually diminish as the backup battery voltage reaches that of the regulation voltage.

Vibra Alerting Device

A vibra alerting device is used for giving silent signal to the user of an incoming call. The device is not placed in the phone but it will be added to a special battery pack. The vibra is controlled with a PWM signal by the MAD via the BTEMP battery terminal.

A 15kohm BSI resistor is needed to detect the vibra battery. It is only used to enable vibra selection in user menu. When alerting, VibraPWM signal is delivered to battery.



IBI Accessories

All accessories which can be connected between the transceiver and the battery or which itself contain the battery, are called IBI accessories.

Either the phone or the IBI accessory can turn the other on, but both possibilities are not allowed in the same accessory.

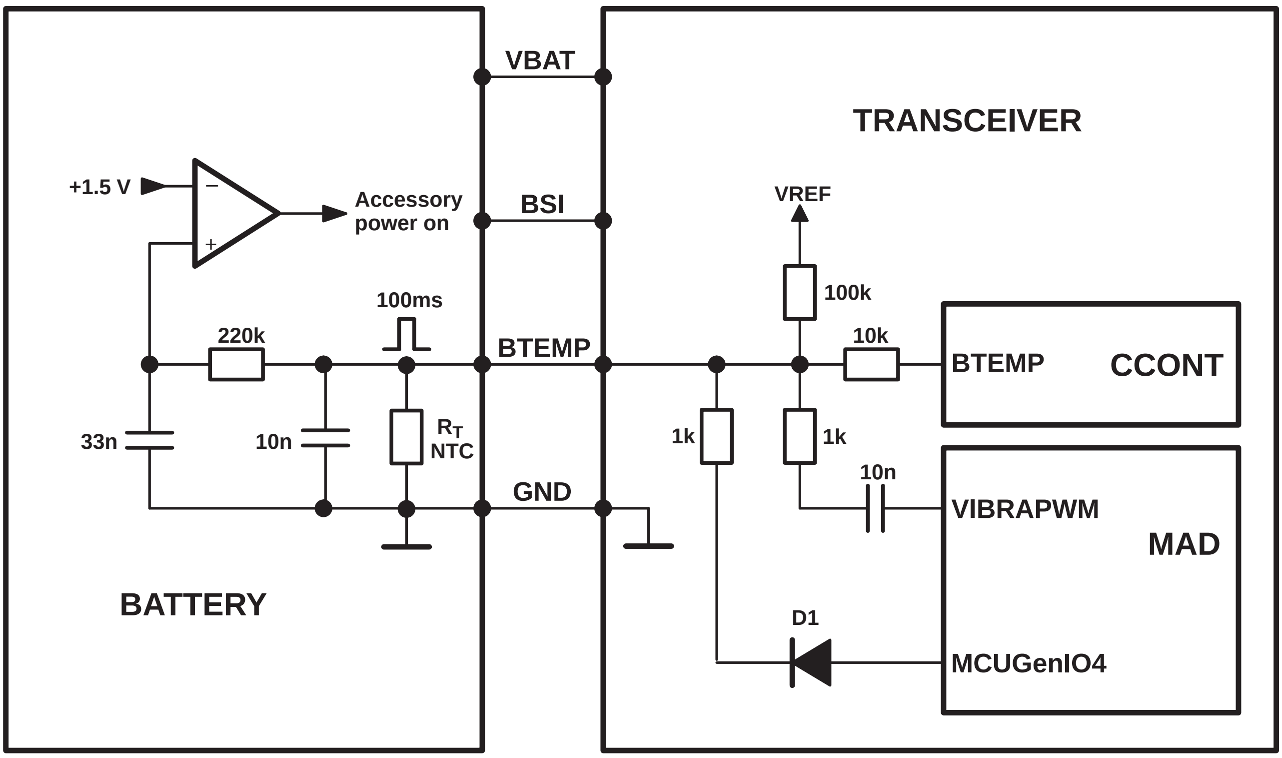
Phone Power–on by IBI

IBI accessory can power the phone on by pulling the BTEMP line up to 3 V.

IBI power–on by phone

Phone can power the IBI accessory on by pulling the BTEMP line up by MCUGenIO4 of MAD2. BTEMP measurement is not possible during this time.

The accessory is commanded back to power–off by MBUS message.



RF Module

Functional Description

This RF module takes care of all RF–functions of the transceiver. RF block diagram has conventional dual conversion receiver and in transmitter there is a upconversion mixer for the final TX–frequency.

Architecture contains three ICs. Most of the functions are horizontally and vertically integrated. UHF functions except power amplifier and VCO are integrated into CRFU3_e1, which is a BiCMOS–circuit suitable for LNA– and mixer–function. Most of the functions are in SUMMA, which also is a BiCMOS–circuit. SUMMA is a IF–circuit including IQ–modulator and PLLs for VHF– and UHF–synthesizers.

Power amplifier is also an ASIC, it is a so called MMIC (monolithic microwave integrated circuit). It has three amplifier stages including input and interstage matchings. Output matching network is external. Also TX gain control is integrated into this chip.

RF block

RF block diagram has conventional dual conversion receiver for GSM and triple conversion receiver for DCS1800. Both receivers use upper side LO drive in the first RF mixer, after that lower side LO drive is used. Because of this there is no need to change I/Q phasing in baseband when receiving band is changed between DCS and GSM.The two receiver chains are combined in 73 MHZ IF so they use same rx–chain from that point down to 13MHz A–D converter. In trans mitter side there are two imagerejection upconversion mixers,one for GSM and one for DCS 1800, for the final TX–frequency. Both use upper side LO drive. Because there is only one external antenna connector used, common for both bands, dualband duplexer that has one common antenna input/output is used.

Architecture contains three ICs. Most of the functions are horizontally and vertically integrated. UHF functions except power amplifier and VCO are integrated
into CRFU3, which is a RF–IC using bipolar process (Ft=25GHz) suitable for 2GHz LNA– and mixer–functions. CRFU3 also includes divide–by–two presca– ler for UHF–VCO. Using this divider it is possible to use only one UHF–VCO running at 2GHz and UHF synthesizer in SUMMA can still use 1GHz LO signal with both systems. The selection between GSM and DCS1800 operation modes in CRFU3 is done with mode selection signal derived from MAD IC in baseband. This signal controls the biasing circuitries of the different RF blocks in CRFU3 so that GSM blocks and DCS1800 blocks are not active at the same time. This way there is no need for extra voltage regulators and the same CCONT regulator–IC can be used as in singlebander DCT3 products
Most of the RF–functions are in SUMMA which is a BiCMOS–circuit.

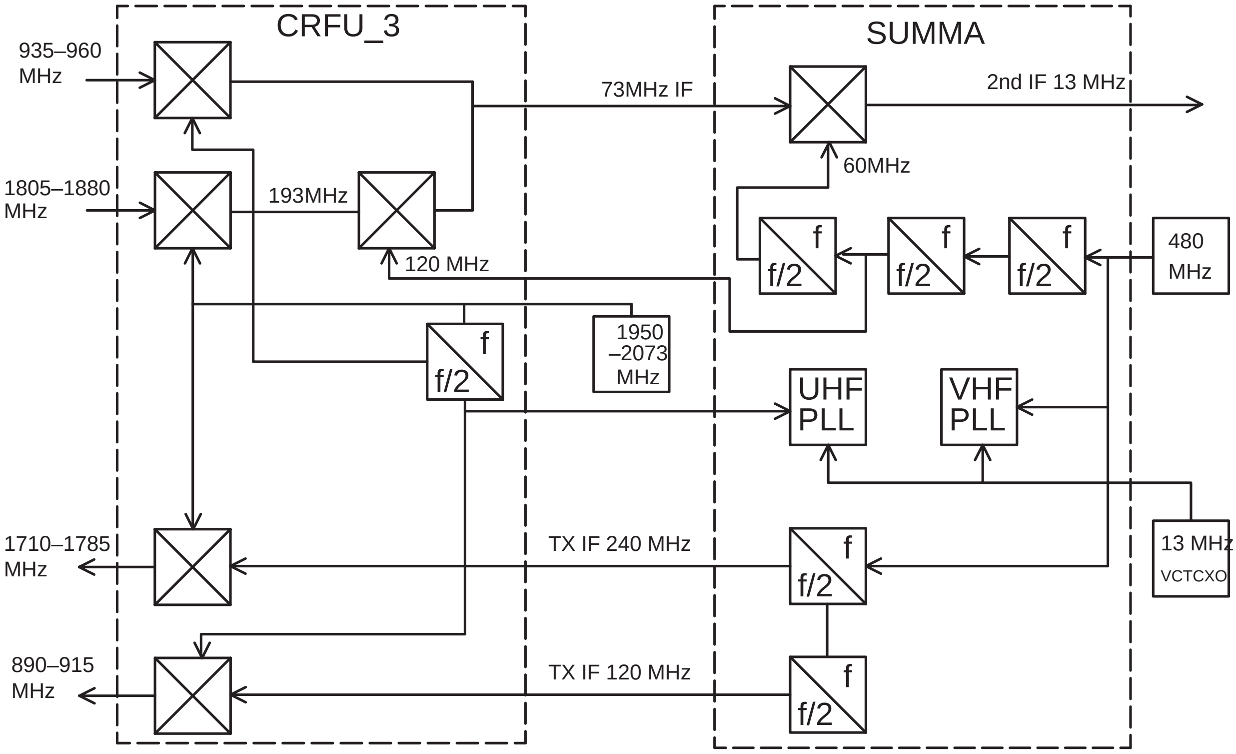
SUMMA is an IF–circuit including IQ–modulator with two buffered outputs ,one for GSM TX IF and one for DCS1800 TXIF, PLLs for VHF– and UHF–synthesizers, RX AGC amplifier and RX mixer for 13 MHz down-conversion. It also includes two operational amplifiers for TX power control loop. There is one common input for power detector voltage and one for TXC–control and two outputs for power control of the PA, one for GSM PA and one for DCS PA. The selection between GSM and DCS1800 operation modes is done via serial bus of SUMMA.

Power amplifiers are also ASICs, called MMIC (monolithic microwave integrated circuit). There are two separate PAs, one for GSM and one for DCS1800. Both PAs include input and interstage matchings. Output matching networks are external for both systems. TX gaincontrol is also integrated into these chips.
See block diagram.

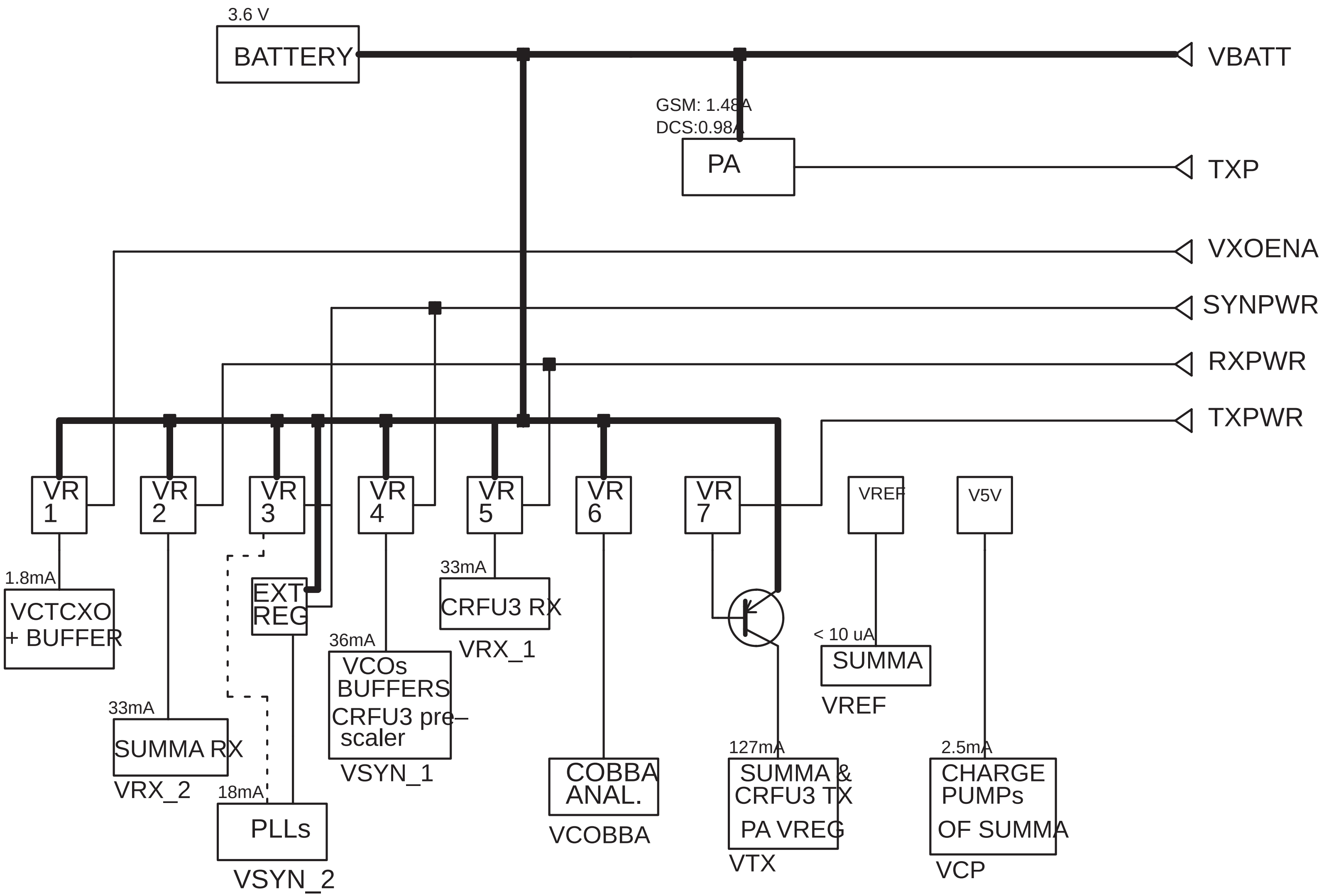
Maximum Ratings

Parameter	Rating
Battery voltage, idle mode	6.0 V
Battery voltage during call, highest power level	5.0 V
Regulated supply voltage	2.8 +/– 3% V
Voltage reference	1.5 +/– 1.5% V
Operating temperature range	–10...+55 deg. C

RF Frequency Plan



Power Distribution Diagram



DC Characteristics

Regulators

Transceiver has got a multi function power management IC, which contains among other functions, also 7 pcs of 2.8 V regulators. All regulators can be controlled individually with 2.8 V logic directly or through control register. Direct controls are used to get fast switching, because regulators are used to enable RF–functions.

Use of the regulators can be seen in the power distribution diagram.

CCONT also provides 1.5 V reference voltage for SUMMA (and for DACs and ADCs in COBBA too).

Control Signals

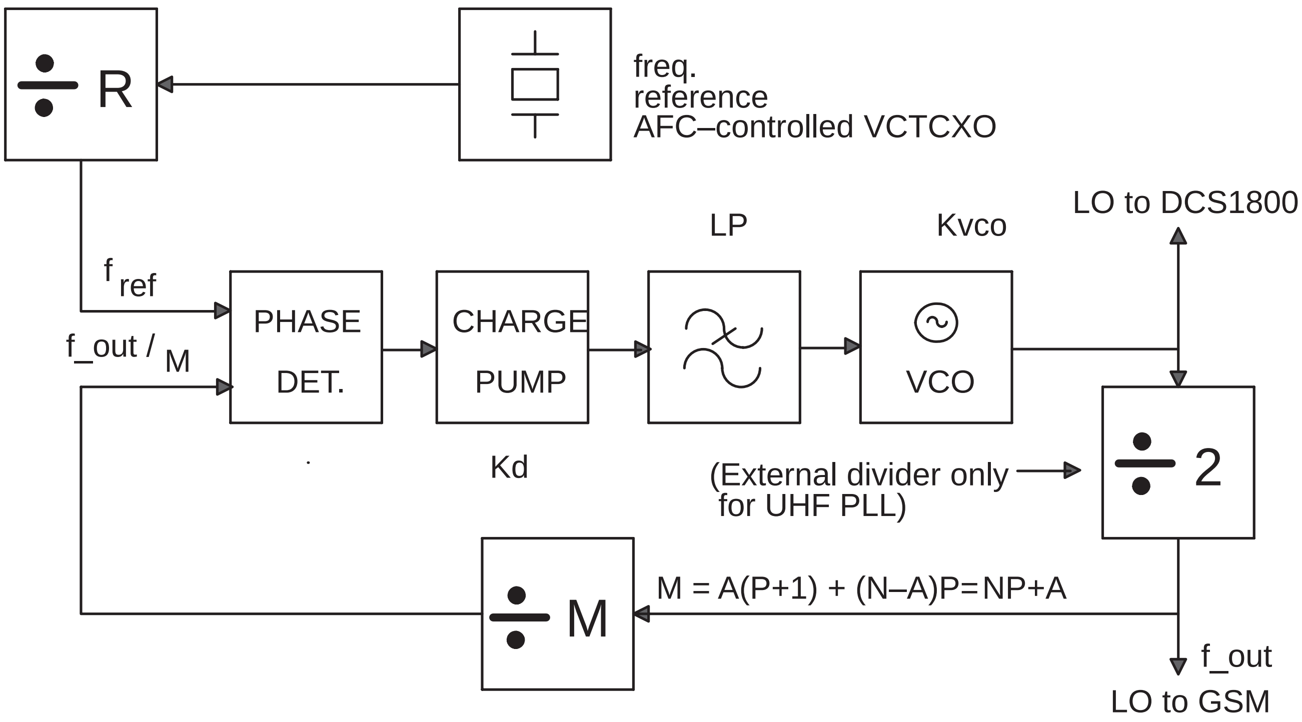
All control signals are coming from MAD and they are 2.8 V logic signals.

Frequency synthesizers

Both UHF– and VHF–VCO are locked with PLLs into stable frequency source, which is a VCTCXO–module (voltage controlled temperature compensated crystal oscillator). Using VCTCXO, it is possible to leave the center frequency and control curve slope calibration away in production if needed.This VCTCXO is running at 13 MHz. Temperature effect is controlled with AFC (automatic frequency control) voltage in order to maintain VCTCXO locked into frequency of the base station. AFC is generated by baseband with a 11 bit DAC in COBBA–ASIC.

UHF PLL is located in SUMMA. There are 64/65 (P/P+1) prescaler, N– and A–divider, reference divider, phase detector and charge pump for the external loop filter. UHF local signal is generated by dividing the UHF–VCO signal (there is only one UHF–VCO module, that is common for both systems, running at 2GHz) by two in CRFU3 prescaler and from that the signal is fed to SUMMA prescaler. Prescaler is a dual modulus divider. Output of the prescaler is fed to N– and A–divider, which produce the input to phase detector. Phase detector compares this signal to reference signal, which is divided with reference divider from VCTCXO output. Output of the phase detector is connected into charge pump, which charges or discharges integrator capacitor in the loop filter depending on the phase of the measured frequency compared to reference frequency. Loop filter filters out the pulses and generates DC to control the frequency of UHF–VCO. Loop filter defines step response of the PLL (settling time) and effects to stability of the loop, that's why integrator capacitor has got a resistor for phase compensation. Other filter components are for sideband rejection.
Dividers are controlled via serial bus. SDATA is for data, SCLK is serial clock for the bus and SENA1 is a latch enable, which stores new data into

dividers.
UHF–synthesizer is the channel synthesizer, so the channel spacing is 200 kHz. When GSM operation is active, 200 kHz reference frequency is used for the phase detector. For DCS1800 operation, 100 kHz reference frequency has to be used.This is because GSM UHF parts use 1GHz signal as an LO which is same as the local signal for the UHF synthesizer and DCS1800 UHF parts use 2GHz signal as an LO, but the UHF synthesizer is locked to 1GHz local signal, which is derived from dividing UHF–VCO signal by two.



VHF PLL is also located into SUMMA. There is 16/17 (P/P+1) dual modulus prescaler, N– and A–dividers, reference divider, phase detector and charge pump for the loop filter. VHF local signal is generated with a discrete VCO–circuit running at 480MHz. VHF PLL is common for GSM and DCS1800. VHF–PLL is locked on fixed frequency (frequency is same for GSM and DCS1800), used reference frequency is 200kHz

Receiver

GSM frontend

GSM receiver is a dual conversion linear receiver. This frontend in CRFU3 rf–asic is activated with mode–selection signal set to high–state. Received RF–signal from the antenna is fed via the duplex filter to LNA (low noise amplifier) in CRFU3. Active parts (RF–transistor and biasing and AGC–step circuitry) are integrated into this chip. Input and output matching networks are external. Gain selection is done with PDATA0 control. Gain step in LNA is activated when RF–level in antenna is about –47 dBm. After the LNA,amplified signal (with low noise level) is fed to bandpass filter, which is a SAW–filter (SAW, surface acoustic wave). Duplex filter and RX interstage bandpass filters together define, how good are the blocking characteristics against spurious signals outside receive band and the protection against spurious responses, mainly the image of the first mixer.

This bandpass filtered signal is then mixed down to 73 MHz, which is first GSM intermediate frequency. 1st mixer is located into CRFU3 ASIC. This integrated mixer is a double balanced Gilbert cell. It is driven balanced. All active parts and biasing are integrated and matching components are external. Because this is an axtive mixer it also amplifies IF–frequency. Also local signal buffering is integrated and upper side injection is used. First local signal is generated with UHF–synthesizer.

DCS1800 frontend

DCS receiver is a triple conversion linear receiver.This frontend in CRFU3 rf–asic is activated with mode–selection signal set to low–state. Received RF–signal from the antenna is fed via the duplex filter to LNA (low noise amplifier) in CRFU3. Active parts (RF–transistor and biasing and AGC–step circuitry) are integrated into this chip. Input and output matching networks are external. Gain selection is done with PDATA0 control. Gain step in LNA is activated when RF–level in antenna is about –47 dBm. After the LNA amplified signal (with low noi–se level) is fed to bandpass filter, which is a SAW. Duplex filter and RX interstage bandpass filters together define, how good are the blocking characteristics against spurious signals outside receive band and the protection against spurious responses.

This bandpass filtered signal is then mixed down to 193 MHz IF, which is first DCS intermediate frequency. 1st mixer is in CRFU3 ASIC. This integrated mixer is a double balanced Gilbert cell. It is driven balanced. All active parts and biasing are integrated and matching components are external. Because this is an axtive mixer it also amplifies IF–frequency. Also local signal buffering is integrated and upper side injection is used. First local signal is generated with UHF–synthesizer.There is a balanced LC–bandpass filter in the output of the first mixer which e.g. attenuates the critical 167MHz spurious and 156,5 MHz half–if frequency. It also matches impedance of 193MHz output to following stage input. After this filter, the 193MHz IF–signal is mixed down to 73MHz IF, which is second

DCS intermediate frequency. This VHF–mixer is also double balanced Gilbert cell and is located into CRFU3. Lower side LO signal is used. This 120MHz lo signal is got from SUMMA–ASIC where it is derived by dividing 480MHz VHFLO signal by four.There is an external lowpass filter for this 120MHz lo signal which attenuates the harmonics (especially 240MHz) so that the critical mixing spurious will be attenuated.

Common Receiver parts for GSM and DCS1800

After the GSM RX–mixer and DCS VHF–mixer, the RX–signal path is common for both systems. This 73MHz IF–signal is bandpass filtered with a selective SAW–filter. From the mixers‘ outputs to IF–circuit input of SUMMA–ASIC, signal path is balanced. IF–filter provides selectivity for channels greater than +/–200 kHz. Also it attenuates image frequency of the following mixer and intermodulating signals. Selectivity is required in this place, because of needed linearity and without filtering adjacent channel interferers would be on too high signal level for the stages following.

Next stage in the receiver chain is an AGC–amplifier. It is integrated into SUMMA–ASIC. AGC gain control is analog. Control voltage for the AGC is generated with DA–converter in COBBA–ASIC in baseband. AGC–stage provides accurate gain control range (min. 57 dB) for the receiver. After the AGC–stage, the 73MHz if–signal is mixed down to 13MHz. The needed 60MHz LO signal is generated in SUMMA by dividing VHF–synthesizer output (480 MHz) by eight .

The following IF–filter is a ceramic bandpass filter at 13 MHz. It attenuates adjacent channels, except for +/– 200 kHz there is not much attenuation. Those +/– 200 kHz interferers are filtered digitally by the baseband. Because of this RX DACs has to be so good, that there is enough dynamic range for the faded 200 kHz interferer. Also the whole RX has to be able to handle signal levels in a linear way. After the 13 MHz filter there is a buffer for the IF–signal, which also converts and amplifies single ended signal from filter to balanced signal for the buffer and AD–converters in COBBA. Buffer in SUMMA has voltage gain of 36 dB and buffer gain setting in COBBA is 0 dB. It is possible to set gainstep (9.5 dB) into COBBA via control bus, if needed.

Transmitter

Transmitter chain consists of IQ–modulator which is common for both systems, two image rejection upconversion mixers, two power amplifiers and a power control loop.

GSM transmitter

I– and Q–signals are generated by baseband in COBBA–ASIC. After post filtering (RC–network) they are fed into IQ–modulator in SUMMA. It generates modulated TX IF–frequency, which is VHF–synthesizer output divided by four, meaning 120 MHz. The TX–amplifier in SUMMA has two selectable gain levels. Output is set to maximum via control register of SUMMA. After SUMMA there is a bandpass LC–filter for noise and harmonic filtering before the signal is fed for upconversion into final TX–frequency in CRFU3. Upconversion mixer in CRFU3 is so called image rejection mixer. It is able to attenuate unwanted sideband in the upconverter output. Mixer itself is a double balanced Gilbert cell. Phase shifters required for image rejection are also integrated. Local signal needed in upconversion is generated by the UHF–synthesizer, but buffers for the mixer are integrated into CRFU3. Output of the upconverter is single ended and requires external matching to 50 ohm impedance.

Next stage is TX interstage filter, which attenuates unwanted signals from the upconverter, mainly LO–leakage and image frequency from the upconverter. Also it attenuates wideband noise. This bandpass filter is a SAW–filter.

After interstage filter, tx–signal is fed to GSM input of the PA, which is a MMIC consisting of three amplifier stages and interstage matchings. It has 50 ohm input, but output requires an external matching network. Gain control is integrated into PA and it is controlled with a power control loop. PA has over 35 dB power gain and it is able to produce 3.0 W into output with 0 dBm input level. Gain control range is over 35 dB to get desired power levels and power ramping up and down. Harmonics generated by the nonlinear PA (class AB) are filtered out with the matching network and lowpass/bandstop filtering in the duplexer. Bandstop is required because of wideband noise located on RX–band. There is a directional coupler connected between PA output and duplex filter input.

DCS1800 transmitter

I– and Q–signal routes from COBBA–ASIC, post filtering and IQ–modulator in SUMMA are common with GSM. In DCS1800, TX–IF frequency is generated by using VHF synthesizer frequency divided by two, meaning 240 MHz. The TX–amplifier in SUMMA has two selectable gain levels. Output (single–ended) is set to maximum via control register of SUMMA. After SUMMA there is a lowpass LC–filter for harmonic filtering before the signal is fed for upconversion into final TX–frequency in CRFU3. Upconversion mixer for DCS is also image rejection mixer. Local signal needed in upconversion is generated by the UHF–synthesizer and buffers for the mixer are integrated into CRFU3. Output of the upconverter is single ended and requires external matching to 50 ohm impedance.

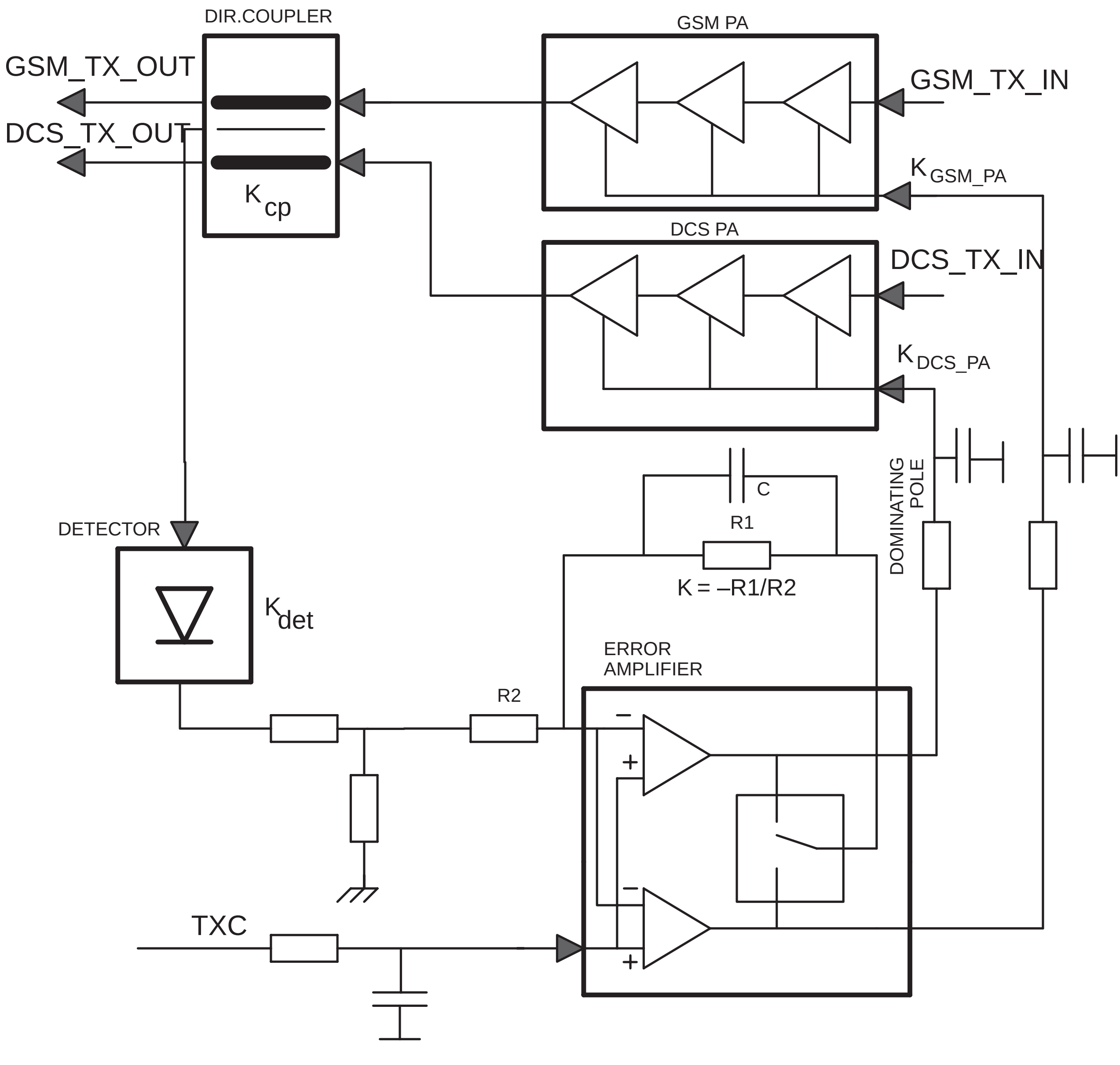
Next stage is TX interstage filter, which attenuates unwanted signals from the upconverter, mainly LO–leakage and image frequency from the upconverter. Also it attenuates wideband noise. This bandpass filter is a SAW filter.

After interstage filter, tx–signal is fed to the input of DCS MMIC PA. It is 50 ohm input, but output requires an external matching network. DCS MMIC PA contains three amplifier stages and interstage matchings. The PA has over 33 dB power gain and it is able to produce 1.9 W into output with 0 dBm input level. Gain control range is over 35 dB to get desired power levels and power ramping up and down. Output matching and duplexer are used for same purposes as in GSM. There is a directional coupler connected between PA output and duplex filter input.

Transmitter power control for GSM and DCS1800

Power control circuitry consists of PA‘s gain control stage, power detector in the PA output and error amplifier in SUMMA–ASIC. There is a directional coupler connected between PA output and duplex filter in both chains, but the power sensing line and detector are common for both bands. It takes a sample from the forward going power with certain ratio. This signal is rectified in a schotky–diode and it produces a DC–signal after RC–filtering. This peak–detector is linear on absolute scale, except it saturates on very low and high power levels, so it produces a S–shape curve.

This detected voltage is compared in the error–amplifier in SUMMA to TXC–voltage, which is generated by DA–converter in COBBA. The output of the error amplifier is fed to PA gaincontrol stage. Because also gaincontrol characteristics in PA are linear in absolute scale, control loop defines a voltage loop, when closed. Closed loop tracks the TXC–voltage. TXC has a raised cosine form ($\cos^4$ – function), which reduces switching transients, when pulsing power up and down. Because dynamic range of the detector is not wide enough to control the power (actually RF output voltage) over the whole range, there is a control named TXP to work under detected levels. Burst is enabled and set to rise with TXP until the output level is high enough for the feedback loop to work. Loop controls the output power via the control pin in PA MMIC to the desired output level and burst has the waveform of TXC–ramps. Because feedback loops could be unstable, this loop is compensated with a dominating pole. This pole decreases gain on higher frequencies to get phase margins high enough.


DIR.COUPLER
GSM PA
GSM_TX_OUT
GSM_TX_IN
DCS_TX_OUT
K cp
K GSM_PA
DCS PA
DCS_TX_IN
K DCS_PA
DOMINATING POLE
C
R1
DETECTOR
K det
K = –R1/R2
ERROR AMPLIFIER
R2
TXC

AGC strategy

AGC–amplifier is used to maintain output level of the receiver to COBBA A/D–converters almost constant AGC has to be set before each received burst and pre–monitoring is used for this. Receiver is switched on roughly xxx us before the burst begins, DSP measures received signal level and adjusts RXC, which controls RX AGC–amplifier or it switches off the LNA with PDATA0 control line if the signal level is too high. This pre–monitoring is done in three phases and this sets the settling times for RX AGC. Pre–monitoring is required because of linear receiver, received signal must be in full swing, no clipping is allowed and because DSP doesn't know, what is the level going to be in next burst.

There is at least 57 dB accurate gain control (continous, analog) and one digital step in LNA. It is typically about 31...33 dB.

RSSI must be measured on range –48...–110 dBm. After –48 dBm level MS reports to base station the same reading.

Because of RSSI–requirements, gain step in LNA is used roughly on –47 dBm RF–level and up to –10 dBm input RF–level accurate AGC is used to set RX output level. LNA is ON (PDATA0 = "0") below –47 dBm. From –47 dBm down to –95 dBm this accurate AGC in SUMMA is used to adjust the gain to desired value. RSSI–function is in DSP, but it works out received signal level by measuring RX IQ–level after all selectivity filtering (meaning IF–filters, ΣΔ±converter and FIR–filter in DSP). So 48 dB accurate AGC dynamic range is required. Remaining 10 dB is for gain variations in RX–chain (for calibration). Below –95 dBm RF–levels, output level of the receiver drops dB by dB. At –95 dBm level output of the receiver gives 50 mVpp. This is the target value for DSP. Below this it drops down to about 9 mVpp @ –110 dBm RF–level.

This strategy is chosen because AGC in SUMMA has to start to roll off early enough, so that it won't saturate in selectivity tests. Also we can't start too early , i.e. with too low receiving levels , because then we will sacrifice the signal to noise ratio and it would require more accurate AGC dynamic range. 50 mVpp target level is set, because RX–DA converter will saturate at 1.4 Vpp. This over 28 dB headroom is required to have margin for +/– 200 kHz faded adjacent channel (ca. 19 dB) and extra 9 dB for pre–monitoring.

Production calibration is done with two RF–levels, LNA gain step is not calibrated. Gain changes in the receiver are taken off from the dynamic range of accurate AGC. Variable gain stage in SUMMA is temperature compensated so that there should be good enough margin in AGC range to cover the gain changes in frontend of the receiver.

AFC function

AFC is used to lock the transceivers clock to frequency of the base station. AFC–voltage is generated in COBBA with 11 bit AD–converter. There is a RC–filter in AFC control line to reduce the noise from the converter. Settling time requirement for the RC–network comes from signalling, how often PSW (pure sine wave) slots occur. They are repeated every 10 frames, meaning that there is PSW in every 46 ms. AFC tracks base station frequency continously, so transceiver has a stable frequency, because there are no rapid changes in VCTCXO –output (changes due to temperature are relatively slow). Settling time requirement comes also from the start up–time allowed. When transceiver is in sleep mode and ”wakes” up to receive mode, there is only about 5 ms for the AFC–voltage to settle. When the first burst comes in system clock has to be settled into +/– 0.1 ppm frequency accuracy. The VCTCXO–module requires about 4 ms to settle into final frequency. Amplitude rises into full swing in about 3 ms, but because frequency settling time is higher, this oscillator must be powered up early enough.

Receiver blocks

RX interstage filter GSM

Parameter	Min.	Typ.	Max.	Unit
Passband	935 – 960			MHz
Insertion loss			3.8	dB
Maximum drive level			+10	dBm

RX interstage filter DCS1800

Parameter	Min.	Typ.	Max.	Unit / notes
Passband	1805 – 1880			MHz
Insertion loss in passband			3.5	dB
Maximum drive level			+10	dBm

GSM UHF–mixer in CRFU3

Parameter	min.	typ.	max.	unit	notes
Input RF–frequency	925		960	MHz	
Output IF–frequency		73		MHz	
Input LO–frequency	998		1033	MHz	
Output resistance (balanced)				ohm	73 MHz Open collector output

DCS1800 UHF–mixer in CRFU3

Parameter	min.	typ.	max.	unit	notes
Input RF–frequency	1805		1880	MHz	
Output IF–frequency		193		MHz	
Input LO–frequency	1998		2073	MHz	
Output resistance (balanced)				ohm	193 MHz Open collector output

Transmitter Blocks

TX interstage filter GSM

Parameter	Min.	Typ.	Max.	Unit
Passband	890 – 915			MHz
Insertion loss			3.5	dB

TX interstage filter DCS1800

Parameter	Min.	Typ.	Max.	Unit
Passband	1710 – 1785			MHz
Insertion loss			3.5	dB

Power amplifier MMIC GSM

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Operating freq. range			890		915	MHz
Supply voltage	Vcc		3.0	3.5	5.0	V
Gain control range (overall dynamic range)		Vpc= 0.5 ... 2.2 V	45			dB

Power amplifier MMIC DCS1800

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Operating freq. range			1710		1785	MHz
Supply voltage	Vcc		3.0	3.5	5.0	V
Gain control range (overall dynamic range)		Vpc= 0.5 ... 2.2 V	45			dB

Synthesizer blocks

VHF VCO

Parameter	Conditions	Rating	Unit/ Notes
Supply voltage, Vcc		2.8 +/– 0.1	V
Supply current, Icc	Vcc = 2.8+/–0.1 V,	< 7	mA
Control voltage, Vc	Vcc = 2.8+/–0.1 V	0.8... 3.7	V
Operating frequency	Vcc = 2.8+/–0.1 V Vc = 2.25 +/– 0.75V	480	MHz
Control voltage sensitivity	Vcc = 2.8+/–0.1V	10 +/– 3	MHz/V
Output power level	Vcc=2.7 V f= 480 MHz	–6.0 min.	dBm
Supply voltage pushing stability	Vcc=2.8 +/– 0.1 V	+/– 2.0	MHz/V max.

UHF PLL

UHF PLL block in SUMMA

Parameter	Min.	Typ.	Max.	Unit/notes
Input frequency range	650		1700	MHz
Reference input frequency			30	MHz
Reference input level	100			mVpp
Reference input impedance		tbd.		

UHF VCO module

Parameter	Conditions	Rating	Unit/ Notes
Supply voltage, Vcc		2.8 +/– 0.1	V
Supply current, Icc	Vcc = 2.8 V, Vc= 2.25 V	< 10	mA
Control voltage, Vc	Vcc = 2.8 V	0.8... 3.7	V
Oscillation frequency	Vcc = 2.8 V Vc = 0.8 V Vc = 3.7 V	 < 1950 > 2073	 MHz MHz

Parameter	Conditions	Rating	Unit/ Notes
Tuning voltage in center frequency	f = 2011,5 MHz	2.25 +/– 0.25	V
Tuning voltage sensitivity in operating frequency range on each spot freq.	Vcc = 2.8 V f= 1950 ... 2073 MHz	60 +/– 8	MHz/V
Output power level	Vcc=2.7 V f= 1950 ... 2073 MHz	–5.0 min.	dBm

UHF local signal input in CRFU3

Parameter	min	typ	max	unit	notes
Input frequency Fpsi	1950		2073	MHz	Fpsi = Fvco
Input level	400		800	mVpp	single ended.

Connections

RF connector and antenna switch

Parameter	Min.	Typ.	Max.	Unit/Notes
Operating frequency range	890		1880	MHz
Insertion loss in GSM band			0.15	dB
Insertion loss in DCS band			0.25	dB
Nominal impedance		50		ohm
VSWR			tbd.	

Signal name	From/To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
VBATT	Battery RF	Voltage	3.0	3.6	5.0/6.0	V	Supply voltage for RF
		Current			2500	mA	
BANDSEL	MAD **CRFU3**	Logic high ”1”	2.0		2.8	V	GSM RX/TX ON DCS OFF
		Logic low ”0”	0		0.8	V	DCS RX/TX ON GSM OFF
		Current			0.1	mA	
		Timing inaccuracy			10	us	
VXOENA	MAD CCONT	Logic high ”1”	2.0		2.8	V	VR1, VR6 in CCONT ON
		Logic low ”0”	0		0.8	V	VR1, VR6 in CCONT OFF
		Current			0.1	mA	
		Timing inaccuracy			10	us	

Signal name	From/To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
SYNPWR	MAD CCONT	Logic high ”1”	2.0		2.8	V	VR3, VR4 in CCONT ON
		Logic low ”0”	0		0.8	V	VR3,VR4 in CCONT OFF
		Current			0.1	mA	
RXPWR	MAD CCONT	Logic high ”1”	2.0		2.8	V	VR2, VR5 in CCONT ON
		Logic low ”0”	0		0.8	V	VR2, VR5 in CCONT OFF
		Current			0.1	mA	
TXPWR	MAD CCONT	Logic high ”1”	2.0		2.8	V	VR7 in CCONT ON
		Logic low ”0”	0		0.8	V	VR7 in CCONT OFF
		Current			0.1	mA	
VREF	CCONT **SUMMA**	Voltage	1.478	1.5	1.523	V	Reference voltage for **SUMMA**
		Current			100	uA	
		Source resistance		10		ohm	
PDATA0	MAD **CRFU3**	Logic high ”1”	2.0		2.8	V	Nominal gain in LNA
		Logic low ”0”	0		0.8	V	Reduced gain in LNA
		Current			0.1	mA	
SENA1	MAD **SUMMA**	Logic high ”1”	2.0		2.8	V	PLL enable
		Logic low ”0”	0		0.8	V	
		Current			50	uA	
		Load capacitance			10	pF	
SDATA	MAD **SUMMA**	Logic high ”1”	2.0		2.8	V	Synthesizer data
		Logic low ”0”	0		0.8	V	
		Load impedance	10			kohm	
		Load capacitance			10	pF	
		Data rate frequency		3.25		MHz	
SCLK	MAD **SUMMA**	Logic high ”1”	2.0		2.8	V	Synthesizer clock
		Logic low ”0”	0		0.8	V	
		Load impedance	10			kohm	
		Load capacitance			10	pF	
		Data rate frequency		3.25		MHz	

Signal name	From/To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
AFC	COBBA VCTCXO	Voltage	0.046		2.254	V	Automatic frequency control signal for VC(TC)XO
		Resolution	11			bits	
		Load resistance (dynamic)	10			kohm	
		Load resistance (static)	1			Mohm	
		Noise voltage			500	uVrms	10...10000Hz
		Settling time			0.5	ms	
RFC	VC(TC)XO MAD	Frequency		13		MHz	High stability clock signal for the logic circuits
		Signal amplitude	0.5	1.0	2.0	Vpp	
		Load resistance	10			kohm	
		Load capacitance			10	pF	
RXIP/ RXIN	**SUMMA** COBBA	Output level		50	1344	mVpp	Differential RX 13 MHz signal to baseband
		Source impedance			tbd.	ohm	
		Load resistance		1		Mohm	
		Load capacitance			tbd.	pF	
TXIP/TXIN	COBBA **SUMMA**	Differential voltage swing	1.022	1.1	1.18	Vpp	Differential in–phase TX baseband signal for the RF modulator
		DC level	0.784	0.8	0.816	V	
		Differential offset voltage (corrected)			+/– 2.0	mV	
		Diff. offset voltage temp. dependence			+/– 1.0	mV	
		Source impedance			200	ohm	
		Load resistance	40			kohm	
		Load capacitance			10	pF	
		DNL			+/– 0.9	LSB	
		INL			+/–1	LSB	
		Group delay mis-smatch			100	ns	

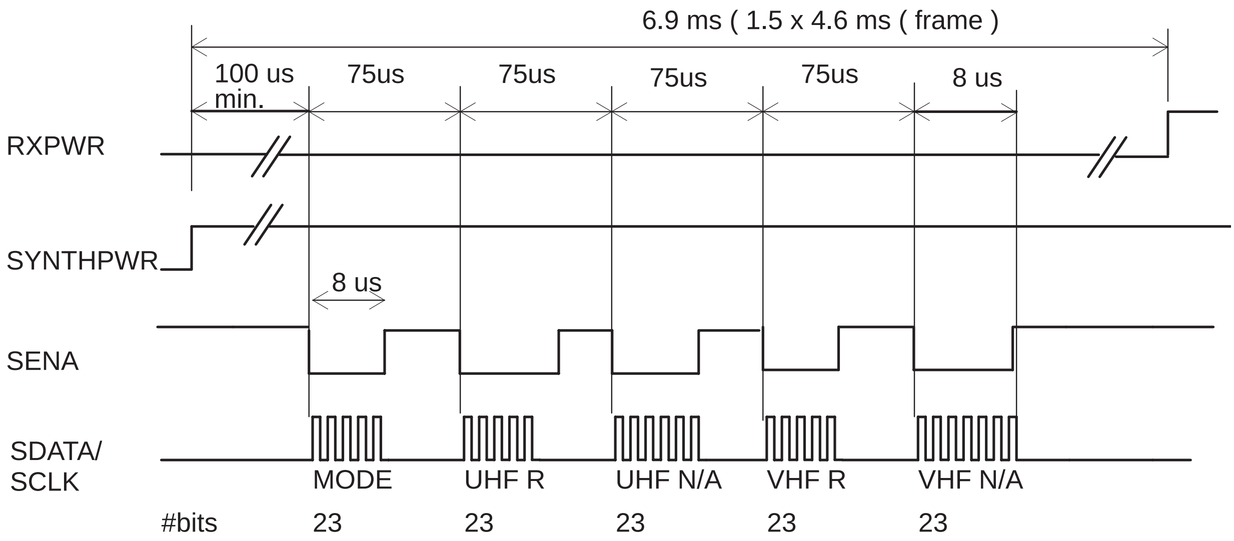
Signal name	From/To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
TXQP/ TXQN	COBBA **SUMMA**	Differential voltage swing	1.022	1.1	1.18	Vpp	Differential quadrature phase TX baseband signal for the RF mod-ulator
		DC level	0.784	0.8	0.816	V	
		Differential offset voltage (corrected)			+/– 2.0	mV	
		Diff. offset voltage temp. dependence			+/– 1.0	mV	
		Source impedance			200	ohm	
		Load resistance	40			kohm	
		Load capacitance			10	pF	
		Resolution	8			bits	
		DNL			+/– 0.9	LSB	
		INL			+/–1	LSB	
		Group delay mis-smatch			100	ns	
TXP	MAD **SUMMA**	Logic high ”1”	2.0		2.8	V	Transmitter power control enable
		Logic low ”0”	0		0.8	V	
		Load Resistance	50			kohm	
		Load Capacitance			10	pF	
		Timing inaccuracy			1	us	
TXC	COBBA **SUMMA**	Voltage Min	0.12		0.18	V	Transmitter power control
		Voltage Max	2.27		2.33	V	
		Vout temperature dependence			10	LSB	
		Source impedance active state			200	ohm	
		Source impedance power down state	high Z				
		Input resistance	10			kohm	
		Input capacitance			10	pF	
		Settling time			10	us	
		Noise level			500	uVrms	0...200 kHz
		Resolution	10			bits	
		DNL			+/–0.9	LSB	
		INL			+/– 4	LSB	
		Timing inaccuracy			1	us	

Signal name	From/To	Parameter	Mini-mum	Typi-cal	Maxi-mum	Unit	Function
RXC	COBBA **SUMMA**	Voltage Min	0.12		0.18	V	Receiver gain control
		Voltage Max	2.27		2.33	V	
		Vout temperature dependence			10	LSB	
		Source impedance active state			200	ohm	
		Source impedance power down state	grounded				
		Input resistance	1			Mohm	
		Input capacitance			10	pF	
		Settling time			10	us	
		Noise level			500	uVrms	0...200 kHz
		Resolution	10			bits	
		DNL			+/–0.9	LSB	
		INL			+/– 4	LSB	

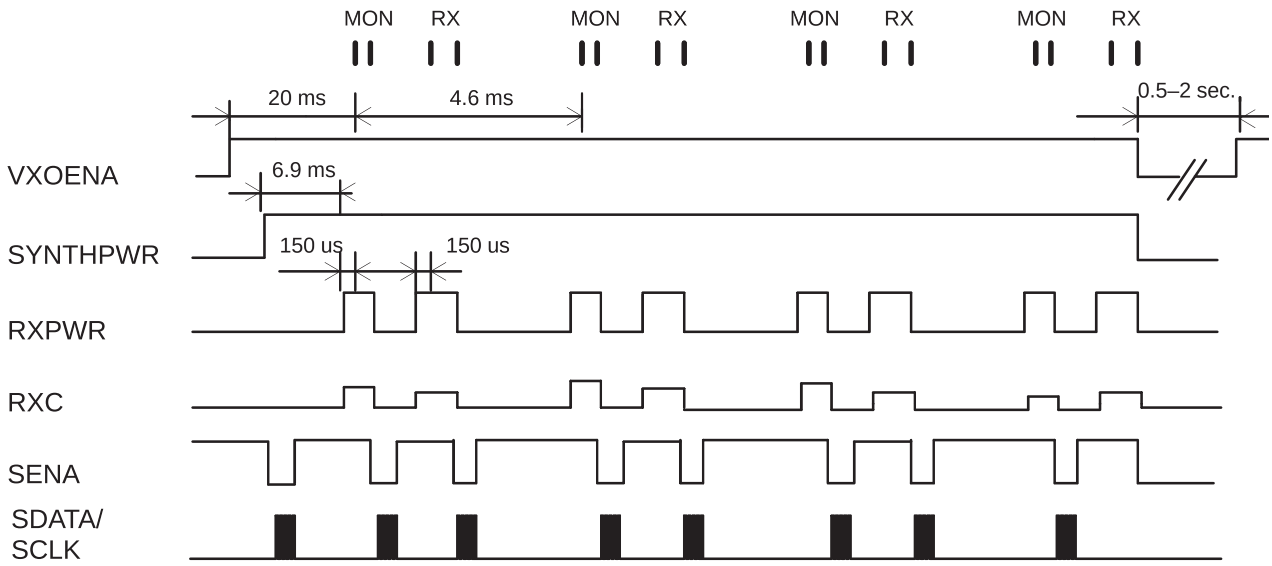
NOTE: Logic controls in low state when RF in power off.

Timings

Synthesizer control timing

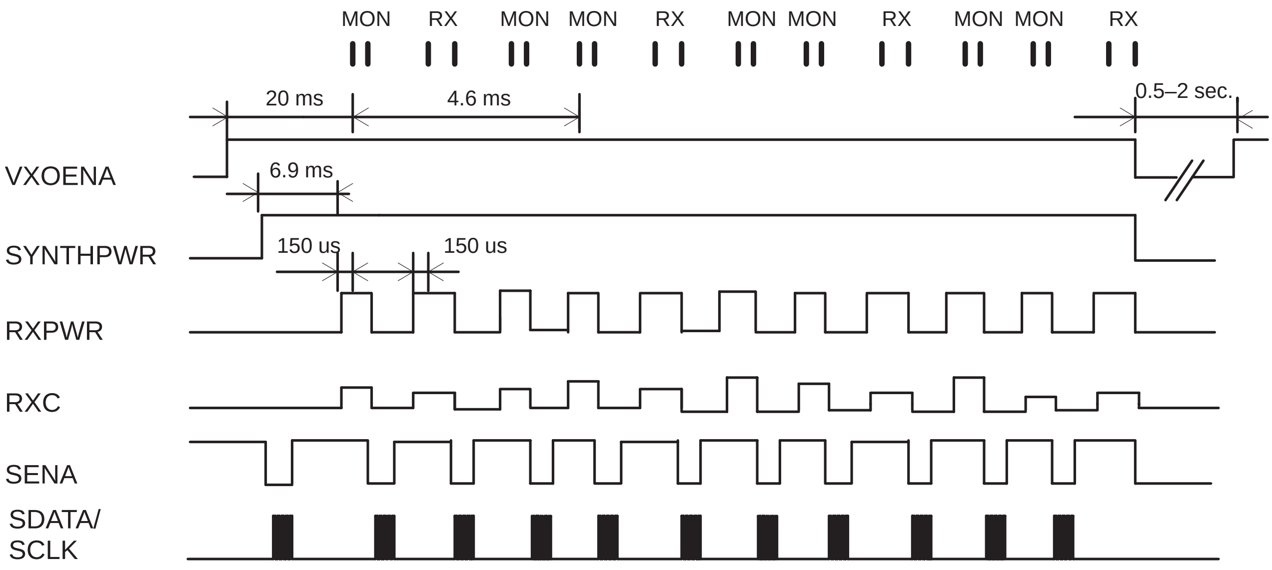


Synthesizer Start–up Timing / clocking

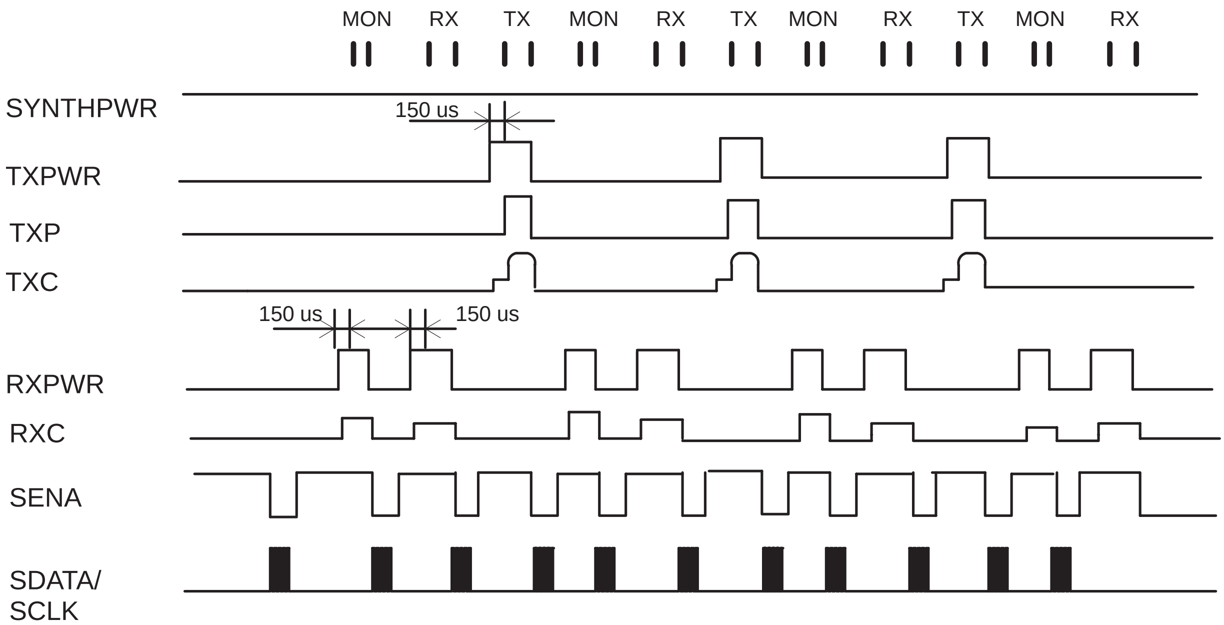


Synthesizer Timing / IDLE,
one monitoring frame,
frame can start also from RX–burst

In case of long list of adjacent channels, there might be two monitoring–bursts/frame. Extra monitoring ”replaces” TX–burst.

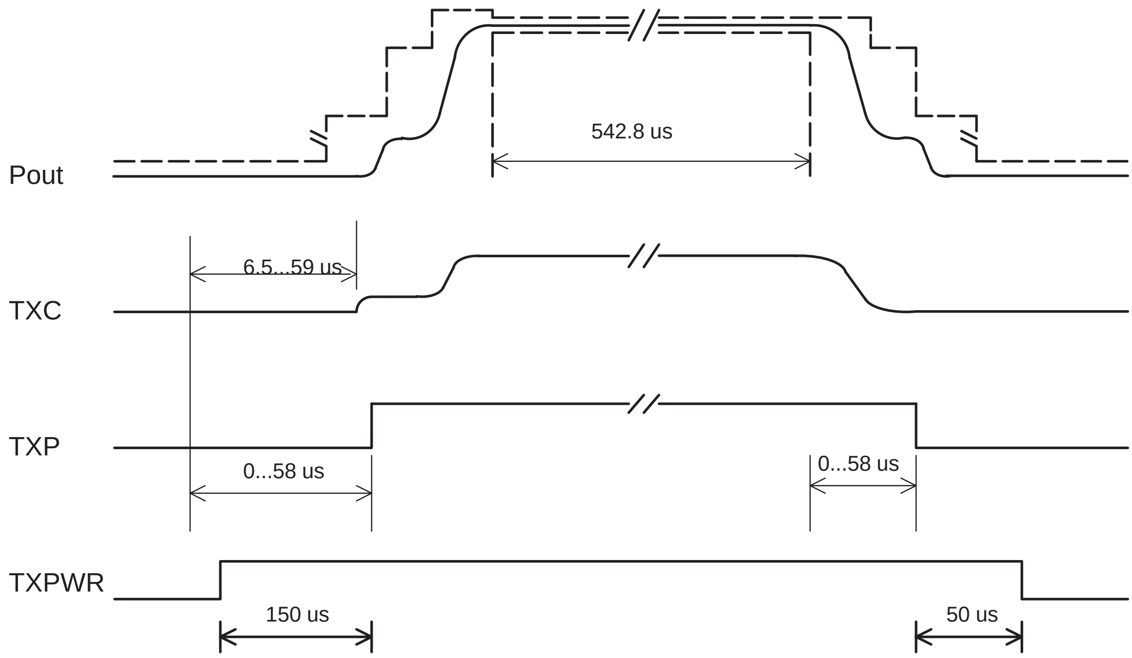


Synthesizer Timing / IDLE 2, frame can start from RX–burst



Synthesizer Timing / traffic channel

Transmitter power switching timing diagram



Synthesizer clocking

Synthesizers are controlled via serial control bus, which consists of SDATA, SCLK and SENA1 signals. These lines form a synchronous data transfer line. SDATA is for the data bits, SCLK is 3.25 MHz clock and SENA1 is latch enable, which stores the data into counters or registers.

Parts list of UG3 (EDMS Issue 6.3) Code: 0201113

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R100	1430826	Chip resistor	680 k	5 % 0.063 W 0402
R102	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R103	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R104	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R109	1620017	Res network 0w06 2x100r j	0404	0404
R113	1430726	Chip resistor	100	5 % 0.063 W 0402
R116	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R118	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R120	1620025	Res network 0w06 2x100k j	0404	0404
R122	1620019	Res network 0w06 2x10k j	0404	0404
R124	1620027	Res network 0w06 2x47r j	0404	0404
R127	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R128	1430718	Chip resistor	47	5 % 0.063 W 0402
R131	1422881	Chip resistor	0.22	5 % 1 W 1218
R136	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R141	1430690	Chip jumper		0402
R143	1430834	Chip resistor	3.3 M	5 % 0.063 W 0402
R144	1430122	Chip resistor	4.7 M	5 % 0.063 W 0603
R152	1430690	Chip jumper		0402
R154	1430325	Chip resistor	2.2 M	5 % 0.063 W 0603
R155	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R160	1620025	Res network 0w06 2x100k j	0404	0404
R161	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R162	1430718	Chip resistor	47	5 % 0.063 W 0402
R201	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R202	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R203	1620029	Res network 0w06 2x4k7 j	0404	0404
R211	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R213	1430690	Chip jumper		0402
R215	1620023	Res network 0w06 2x47k j	0404	0404
R252	1430740	Chip resistor	330	5 % 0.063 W 0402
R254	1620027	Res network 0w06 2x47r j	0404	0404
R256	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R257	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R259	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R260	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R261	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R263	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R265	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R267	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R268	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R270	1620025	Res network 0w06 2x100k j	0404	0404
R308	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402

R401	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R402	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R403	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R404	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R405	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R406	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R411	1430760	Chip resistor	1.8 k	5 % 0.063 W 0402
R413	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R500	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R501	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R503	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R504	1430700	Chip resistor	10	5 % 0.063 W 0402
R507	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R508	1430690	Chip jumper		0402
R509	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R510	1430700	Chip resistor	10	5 % 0.063 W 0402
R511	1430722	Chip resistor	68	5 % 0.063 W 0402
R512	1430728	Chip resistor	120	5 % 0.063 W 0402
R513	1430724	Chip resistor	82	5 % 0.063 W 0402
R514	1430738	Chip resistor	270	5 % 0.063 W 0402
R515	1430742	Chip resistor	390	5 % 0.063 W 0402
R516	1430740	Chip resistor	330	5 % 0.063 W 0402
R517	1430706	Chip resistor	15	5 % 0.063 W 0402
R518	1430740	Chip resistor	330	5 % 0.063 W 0402
R520	1430691	Chip resistor	2.2	5 % 0.063 W 0402
R521	1430691	Chip resistor	2.2	5 % 0.063 W 0402
R550	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R560	1430752	Chip resistor	820	5 % 0.063 W 0402
R561	1430740	Chip resistor	330	5 % 0.063 W 0402
R562	1430740	Chip resistor	330	5 % 0.063 W 0402
R563	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R564	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R565	1430726	Chip resistor	100	5 % 0.063 W 0402
R600	1430744	Chip resistor	470	5 % 0.063 W 0402
R601	1430740	Chip resistor	330	5 % 0.063 W 0402
R602	1430744	Chip resistor	470	5 % 0.063 W 0402
R603	1430730	Chip resistor	150	5 % 0.063 W 0402
R604	1620029	Res network 0w06 2x4k7 j	0404	0404
R605	1430700	Chip resistor	10	5 % 0.063 W 0402
R606	1430734	Chip resistor	220	5 % 0.063 W 0402
R607	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R608	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R609	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R611	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R612	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R614	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R615	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402

R616	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R620	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R621	1430732	Chip resistor	180	5 % 0.063 W 0402
R622	1430718	Chip resistor	47	5 % 0.063 W 0402
R623	1430718	Chip resistor	47	5 % 0.063 W 0402
R624	1820031	NTC resistor	330	10 % 0.12 W 0805
R650	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R652	1430730	Chip resistor	150	5 % 0.063 W 0402
R654	1430700	Chip resistor	10	5 % 0.063 W 0402
R655	1430730	Chip resistor	150	5 % 0.063 W 0402
R656	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R657	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R658	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R659	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R660	1430714	Chip resistor	33	5 % 0.063 W 0402
R670	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R671	1430700	Chip resistor	10	5 % 0.063 W 0402
R672	1430716	Chip resistor	39	5 % 0.063 W 0402
R674	1430690	Chip jumper		0402
R675	1430726	Chip resistor	100	5 % 0.063 W 0402
R676	1430726	Chip resistor	100	5 % 0.063 W 0402
R677	1430728	Chip resistor	120	5 % 0.063 W 0402
R678	1430700	Chip resistor	10	5 % 0.063 W 0402
R690	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R691	1430746	Chip resistor	560	5 % 0.063 W 0402
R692	1430706	Chip resistor	15	5 % 0.063 W 0402
R700	1430691	Chip resistor	2.2	5 % 0.063 W 0402
R702	1430690	Chip jumper		0402
R703	1430702	Chip resistor	12	5 % 0.063 W 0402
R704	1430702	Chip resistor	12	5 % 0.063 W 0402
C100	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C101	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C102	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C103	2604127	Tantalum cap.	1.0 u	20 % 35 V 3.5x2.8x1.9
C104	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C105	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C106	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C107	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C108	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C109	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C110	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C112	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C113	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C114	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C115	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C117	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C118	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402

C119	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C120	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C121	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C122	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C127	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C128	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C129	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C130	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C131	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C132	2312403	Ceramic cap.	2.2 u	10 % 10 V 1206
C133	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C140	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C141	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C142	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C143	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C146	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C147	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C150	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C151	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C152	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C153	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C154	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C156	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C157	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C158	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C160	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C161	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C201	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C202	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C203	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C204	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C205	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C206	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C207	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C208	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C209	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C211	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C212	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C213	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C221	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C231	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C247	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C248	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C249	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C251	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C252	2312296	Ceramic cap.		Y5 V 1210
C253	2320131	Ceramic cap.	33 n	10 % 16 V 0603

C254	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C255	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C256	2312296	Ceramic cap.		Y5 V 1210
C257	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C258	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C260	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C261	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C262	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C263	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C264	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C265	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C266	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C268	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C269	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C271	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C272	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C311	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C312	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C313	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C314	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C315	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C400	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C401	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C402	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C403	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C404	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C405	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C406	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C501	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C502	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C505	2320516	Ceramic cap.	1.5 p	0.25 % 50 V 0402
C506	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C507	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C508	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C509	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C510	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C511	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C512	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C514	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C515	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C516	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C517	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C518	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C519	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C520	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C521	2320570	Ceramic cap.	270 p	5 % 50 V 0402
C522	2320546	Ceramic cap.	27 p	5 % 50 V 0402

C523	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C524	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C525	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C526	2320629	Ceramic cap.		50 V 0402
C527	2320629	Ceramic cap.		50 V 0402
C528	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C529	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C530	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C531	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C532	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C533	2320120	Ceramic cap.	22 n	10 % 25 V 0603
C534	2320748	Ceramic cap.	1.5 n	10 % 50 V 0402
C535	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C536	2320558	Ceramic cap.	82 p	5 % 50 V 0402
C537	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C539	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C540	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C541	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C542	2312921	Ceramic cap.	1.8 n	5 % 50 V 1206
C544	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C545	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C546	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C547	2320582	Ceramic cap.	820 p	5 % 50 V 0402
C548	2320514	Ceramic cap.	1.2 p	0.25 % 50 V 0402
C549	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C550	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C551	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C552	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C553	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C555	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C557	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C560	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C561	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C562	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C563	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C564	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C566	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C567	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C568	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C569	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C571	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C572	2320621	Ceramic cap.	0.5 p	0.25 % 50 V 0402
C573	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C574	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C575	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C576	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C577	2320540	Ceramic cap.	15 p	5 % 50 V 0402

C579	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C580	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C581	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C582	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C583	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C584	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C585	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C587	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C588	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C600	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C601	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C602	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C603	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C604	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C605	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C606	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C607	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C608	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C609	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C610	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C611	2320738	Ceramic cap.	470 p	10 % 50 V 0402
C612	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C613	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C614	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C615	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C616	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C617	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C618	2320483	Ceramic cap.	68 n	10 % 16 V 0603
C619	2320483	Ceramic cap.	68 n	10 % 16 V 0603
C650	2310167	Ceramic cap.	1.0 n	5 % 50 V 1206
C651	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C656	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C657	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C658	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C659	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C660	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C661	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C663	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C664	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C665	2320748	Ceramic cap.	1.5 n	10 % 50 V 0402
C667	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C668	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C669	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C670	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C671	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C680	2611711	Tantalum cap.	330 u	10 % 10 V 7.0x6.0x3.5
C682	2611711	Tantalum cap.	330 u	10 % 10 V 7.0x6.0x3.5

C690	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C691	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C692	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C702	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C703	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C705	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C708	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C713	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C714	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C715	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C718	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C719	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C721	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C722	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C723	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C724	2610024	Tantalum cap.	2.2 u	20 % 16 V 3.2x1.6x1.6
C729	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C750	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C751	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C752	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
L103	3203701	Ferrite bead 33r/100mhz	0805	0805
L104	3203701	Ferrite bead 33r/100mhz	0805	0805
L105	3203701	Ferrite bead 33r/100mhz	0805	0805
L106	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L107	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L108	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L500	3645207	Chip coil	56 n	2 % Q=38/200 MHz 0603
L501	3645207	Chip coil	56 n	2 % Q=38/200 MHz 0603
L502	3645055	Chip coil	120 n	2 % Q=50/250 MHz 0805
L503	3645057	Chip coil	82 n	2 % Q=65/500 MHz 0805
L504	3645057	Chip coil	82 n	2 % Q=65/500 MHz 0805
L506	3641546	Chip coil	82 n	10 % Q=40/150 MHz 0805
L507	3641548	Chip coil	100 n	10 % Q=40/150 MHz 0805
L509	3641626	Chip coil	220 n	2 % Q=30/100 MHz 0805
L510	3641626	Chip coil	220 n	2 % Q=30/100 MHz 0805
L511	3645209	Chip coil	33 n	2 % Q=40/250 MHz 0603
L512	3646003	Chip coil	2 n	Q=30/800M 0402
L513	3646003	Chip coil	2 n	Q=30/800M 0402
L516	3645001	Chip coil	4 n	10 % Q=10/100 MHz 0603
L560	3203705	Ferrite bead 0.015r 42r/100m 0805		0805
L561	3645157	Chip coil	100 n	10 % Q=12/100 MHz 0603
L565	3645055	Chip coil	120 n	2 % Q=50/250 MHz 0805
L570	3646005	Chip coil	2 n	Q=29/800M 0402
L601	3641334	Chip coil	270 n	5 % Q=28/25 MHz 1008
L652	3641206	Chip coil		10% Q=25/7.96 MHz 1008
L653	3645157	Chip coil	100 n	10 % Q=12/100 MHz 0603
L654	3645157	Chip coil	100 n	10 % Q=12/100 MHz 0603

L655	3645157	Chip coil	100 n	10 % Q=12/100 MHz 0603
L656	3645129	Chip coil	18 n	5 % Q=8/100M 0603
L657	3645205	Chip coil	22 n	5 % Q=30/800M 0603
L658	3203709	Ferrite bead 0.5r 120r/100m 0402		0402
L659	3203709	Ferrite bead 0.5r 120r/100m 0402		0402
L660	3203709	Ferrite bead 0.5r 120r/100m 0402		0402
L662	3203709	Ferrite bead 0.5r 120r/100m 0402		0402
L663	3203709	Ferrite bead 0.5r 120r/100m 0402		0402
B100	4510159	Crystal	32.768 k	+–20PPM
G550	4350147	Vco 1950–2073mhz 2.8v 10ma		
G650	4510213	VCTCXO	13 M	+–5PPM 2.8V GSM/PCN
G660	4350145	Vco 480mhz 2.8v 7ma 9.0x7.0x1.7		
F100	5119019	SM, fuse f 1.5a 32v 0603		
Z500	4511057	Saw filter	947.5+–12.5 M	/3.6DB 4X4
Z501	4511055	Saw filter	1842.5+–37.5 M	3.1x3.1
Z560	4512077	Dupl 890–960/1710–1880mhz	24x20	24x20
Z574	4511015	Saw filter	902.5+–12.5 M	/3.8DB 4X4
Z575	4511063	Saw filter	1747.5+–37.5 M	
Z600	4511061	Saw filter	73+–0.09 M	14.2x8.4
Z601	4510009	Cer.filt 13+–0.09mhz 7.2x3.2		7.2x3.2
T500	3640413	Transf balun 1.8ghz+/–100mhz 1206		1206
V100	1825005	Chip varistor vwm14v vc30v 0805		0805
V102	4113651	Trans. supr.	QUAD	6 V SOT23–5
V103	4113601	Emi filter emif01–5250sc5 sot23–5		SOT23–5
V104	4113651	Trans. supr.	QUAD	6 V SOT23–5
V105	4113651	Trans. supr.	QUAD	6 V SOT23–5
V111	4210099	Transistor		SCT595
V112	4219904	Transistor x 2	UMX1	npn 40 V SOT363
V116	4110067	Schottky diode	MBR0520L	20 V 0.5 A SOD123
V250	4210100	Transistor	BC848W	npn 30 V SOT323
V401	4210052	Transistor	DTC114EE	npn RB V EM3
V402	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V560	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V600	4210132	Transistor		SOT323
D200	4370415	Mad2 rom4 v14 f721727 c10 tqfp176		TQFP176
D210	4340509	IC, flash mem.		TSOP48
D221	4340397	IC, SRAM		STSOP3
D230	4340357	IC, EEPROM		SO8
D402	4340369	IC, dual bus buffer sso	TC7W126FU	SSOP8
N100	4370391	Ccont2h dct3 bb asic tqfp64		TQFP64
N101	4370165	Chaps charger control so16		SO16
N201	4340413	IC, regulator	TK11230BMC	3.0 V SOT23L
N250	4370363	Cobba_gj b09 bb asic tqfp64		TQFP64
N300	4113631	Esd array10 ip401		4CV24–45R SSOP2SSOP24
N400	4860031	Tfdu4100 irda tx/rx>2.7v 115kbits		115KBITS

N500	4370407	Crfu3 rf asic gsm/pcn e1 tqfp–48	TQFP–48
N501	4370451	Rf9117e6 pw amp 890–915mhz	
N502	4370453	Rf9118e6 pw amp 1710–1785mhz edss	EDSS
N600	4370351	Summa v2 rx,tx,pll,pcontr. tqfp48	TQFP48
N620	4340335	IC, regulator TK11228AM	SSO6
S301	5219005	IC, SWsp–no 30vdc 50ma smSW TACT	SMD
S302	5219005	IC, SWsp–no 30vdc 50ma smSW TACT	SMD
X100	5469061	SM, system conn 6af+3dc+mic+jack	
X101	5469069	SM, batt conn 2pol spr p3.5 100v	100V2A
X102	5469069	SM, batt conn 2pol spr p3.5 100v	100V2A
X300	5460021	SM, conn 2x14m spring p1.0 pcb/p	PCB/PCB
X302	5409033	Sim card reader ccm04–5004 2x3smd	2x3smd
X560	5429007	SM, coax conn m sw 50r 0.4–2ghz	
A510	9517019	Pa–can dmc01137	
	9854212	PCB UG3 123.3X41.0X0.9 M6 4/PA	

Parts list of UG3MA (EDMS Issue 1.1) Code: 0201380

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R100	1430826	Chip resistor	680 k	5 % 0.063 W 0402
R102	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R103	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R104	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R109	1620017	Res network 0w06 2x100r j	0404	0404
R113	1430726	Chip resistor	100	5 % 0.063 W 0402
R116	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R118	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R120	1620025	Res network 0w06 2x100k j	0404	0404
R122	1620019	Res network 0w06 2x10k j	0404	0404
R124	1620027	Res network 0w06 2x47r j	0404	0404
R127	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R128	1430718	Chip resistor	47	5 % 0.063 W 0402
R131	1422881	Chip resistor	0.22	5 % 1 W 1218
R136	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R141	1430690	Chip jumper		0402
R143	1430834	Chip resistor	3.3 M	5 % 0.063 W 0402
R144	1430122	Chip resistor	4.7 M	5 % 0.063 W 0603
R152	1430690	Chip jumper		0402
R154	1430325	Chip resistor	2.2 M	5 % 0.063 W 0603
R155	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R160	1620025	Res network 0w06 2x100k j	0404	0404
R161	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R162	1430718	Chip resistor	47	5 % 0.063 W 0402
R201	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R202	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R203	1620029	Res network 0w06 2x4k7 j	0404	0404
R211	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R213	1430690	Chip jumper		0402
R215	1620023	Res network 0w06 2x47k j	0404	0404
R252	1430740	Chip resistor	330	5 % 0.063 W 0402
R254	1620027	Res network 0w06 2x47r j	0404	0404
R256	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R257	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R259	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R260	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R261	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R263	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R265	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R267	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R268	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R270	1620025	Res network 0w06 2x100k j	0404	0404
R308	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402

R401	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R402	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R403	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R404	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R405	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R406	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R411	1430760	Chip resistor	1.8 k	5 % 0.063 W 0402
R413	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R500	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R501	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R503	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R504	1430700	Chip resistor	10	5 % 0.063 W 0402
R507	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R508	1430690	Chip jumper		0402
R509	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R510	1430700	Chip resistor	10	5 % 0.063 W 0402
R511	1430722	Chip resistor	68	5 % 0.063 W 0402
R512	1430728	Chip resistor	120	5 % 0.063 W 0402
R513	1430724	Chip resistor	82	5 % 0.063 W 0402
R514	1430738	Chip resistor	270	5 % 0.063 W 0402
R515	1430734	Chip resistor	220	5 % 0.063 W 0402
R516	1430740	Chip resistor	330	5 % 0.063 W 0402
R517	1430706	Chip resistor	15	5 % 0.063 W 0402
R518	1430740	Chip resistor	330	5 % 0.063 W 0402
R550	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R560	1430752	Chip resistor	820	5 % 0.063 W 0402
R561	1430740	Chip resistor	330	5 % 0.063 W 0402
R562	1430740	Chip resistor	330	5 % 0.063 W 0402
R563	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R564	1430766	Chip resistor	3.9 k	5 % 0.063 W 0402
R565	1430726	Chip resistor	100	5 % 0.063 W 0402
R600	1430744	Chip resistor	470	5 % 0.063 W 0402
R601	1430740	Chip resistor	330	5 % 0.063 W 0402
R602	1430744	Chip resistor	470	5 % 0.063 W 0402
R603	1430730	Chip resistor	150	5 % 0.063 W 0402
R604	1620029	Res network 0w06 2x4k7 j	0404	0404
R605	1430700	Chip resistor	10	5 % 0.063 W 0402
R606	1430734	Chip resistor	220	5 % 0.063 W 0402
R607	1430784	Chip resistor	15 k	5 % 0.063 W 0402
R608	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R609	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R611	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R612	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R614	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R615	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R616	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R620	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402

R621	1430732	Chip resistor	180	5 % 0.063 W 0402
R622	1430718	Chip resistor	47	5 % 0.063 W 0402
R623	1430718	Chip resistor	47	5 % 0.063 W 0402
R624	1820031	NTC resistor	330	10 % 0.12 W 0805
R650	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R652	1430730	Chip resistor	150	5 % 0.063 W 0402
R654	1430700	Chip resistor	10	5 % 0.063 W 0402
R655	1430730	Chip resistor	150	5 % 0.063 W 0402
R656	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R657	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R658	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R659	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R660	1430714	Chip resistor	33	5 % 0.063 W 0402
R670	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R671	1430700	Chip resistor	10	5 % 0.063 W 0402
R672	1430716	Chip resistor	39	5 % 0.063 W 0402
R674	1430690	Chip jumper		0402
R675	1430726	Chip resistor	100	5 % 0.063 W 0402
R676	1430726	Chip resistor	100	5 % 0.063 W 0402
R677	1430728	Chip resistor	120	5 % 0.063 W 0402
R678	1430700	Chip resistor	10	5 % 0.063 W 0402
R690	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R691	1430746	Chip resistor	560	5 % 0.063 W 0402
R692	1430706	Chip resistor	15	5 % 0.063 W 0402
R700	1430691	Chip resistor	2.2	5 % 0.063 W 0402
R702	1430690	Chip jumper		0402
R703	1430702	Chip resistor	12	5 % 0.063 W 0402
R704	1430702	Chip resistor	12	5 % 0.063 W 0402
C100	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C101	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C102	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C103	2604127	Tantalum cap.	1.0 u	20 % 35 V 3.5x2.8x1.9
C104	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C105	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C106	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C107	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C108	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C109	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C110	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C112	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C113	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C114	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C115	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C117	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C118	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C119	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C120	2320620	Ceramic cap.	10 n	5 % 16 V 0402

C121	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C122	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C127	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C128	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C129	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C130	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C131	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C132	2312403	Ceramic cap.	2.2 u	10 % 10 V 1206
C133	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C140	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C141	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C142	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C143	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C146	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C147	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C150	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C151	2312211	Ceramic cap.	3.3 u	10 % 0805
C152	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C153	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C154	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C156	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C157	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C158	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C160	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C161	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C201	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C202	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C203	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C204	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C205	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C206	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C207	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C208	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C209	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C211	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C212	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C213	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C221	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C231	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C247	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C248	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C249	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C251	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C252	2312296	Ceramic cap.		Y5 V 1210
C253	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C254	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C255	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805

C256	2312296	Ceramic cap.		Y5 V 1210
C257	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C258	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C260	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C261	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C262	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C263	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C264	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C265	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C266	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C268	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C269	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C271	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C272	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C311	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C312	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C313	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C314	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C315	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C400	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C401	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C402	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C403	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C404	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C405	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C406	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C501	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C502	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C505	2320516	Ceramic cap.	1.5 p	0.25 % 50 V 0402
C506	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C507	2320518	Ceramic cap.	1.8 p	0.25 % 50 V 0402
C508	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C509	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C510	2320752	Ceramic cap.	2.2 n	10 % 50 V 0402
C511	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C512	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C514	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C515	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C516	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C517	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C518	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C519	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C520	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C521	2320570	Ceramic cap.	270 p	5 % 50 V 0402
C522	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C523	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C524	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402

C525	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C526	2320629	Ceramic cap.		50 V 0402
C527	2320629	Ceramic cap.		50 V 0402
C528	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C529	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C530	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C531	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C532	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C533	2320120	Ceramic cap.	22 n	10 % 25 V 0603
C534	2320748	Ceramic cap.	1.5 n	10 % 50 V 0402
C535	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C536	2320558	Ceramic cap.	82 p	5 % 50 V 0402
C537	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C539	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C540	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C541	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C542	2312921	Ceramic cap.	1.8 n	5 % 50 V 1206
C544	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C545	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C546	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C547	2320582	Ceramic cap.	820 p	5 % 50 V 0402
C548	2320514	Ceramic cap.	1.2 p	0.25 % 50 V 0402
C549	2320604	Ceramic cap.	18 p	5 % 50 V 0402
C550	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C551	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C552	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C553	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C555	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C557	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C560	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C561	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C562	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C563	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C564	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C566	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C567	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C568	2320556	Ceramic cap.	68 p	5 % 50 V 0402
C569	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C571	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C572	2320621	Ceramic cap.	0.5 p	0.25 % 50 V 0402
C573	2320598	Ceramic cap.	3.9 n	5 % 50 V 0402
C574	2320520	Ceramic cap.	2.2 p	0.25 % 50 V 0402
C575	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C576	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C577	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C579	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C580	2320554	Ceramic cap.	56 p	5 % 50 V 0402

C581	2320778	Ceramic cap.	10 n	10 % 16 V 0402
C582	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C583	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C584	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C585	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C587	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C588	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C600	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C601	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C602	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C603	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C604	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C605	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C606	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C607	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C608	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C609	2320779	Ceramic cap.	100 n	10 % 16 V 0603
C610	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C611	2320738	Ceramic cap.	470 p	10 % 50 V 0402
C612	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C613	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C614	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C615	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C616	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C617	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C618	2320483	Ceramic cap.	68 n	10 % 16 V 0603
C619	2320483	Ceramic cap.	68 n	10 % 16 V 0603
C650	2310167	Ceramic cap.	1.0 n	5 % 50 V 1206
C651	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C656	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C657	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C658	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C659	2320744	Ceramic cap.	1.0 n	10 % 50 V 0402
C660	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C661	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C663	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C664	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C665	2320748	Ceramic cap.	1.5 n	10 % 50 V 0402
C667	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C668	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C669	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C670	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C671	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C680	2611711	Tantalum cap.	330 u	10 % 10 V 7.0x6.0x3.5
C682	2611711	Tantalum cap.	330 u	10 % 10 V 7.0x6.0x3.5
C690	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C691	2320550	Ceramic cap.	39 p	5 % 50 V 0402

C692	2320522	Ceramic cap.	2.7 p	0.25 % 50 V 0402
C695	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C696	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C702	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C703	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C705	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C708	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C713	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C714	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C715	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C718	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C719	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C721	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
C722	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C723	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C724	2610024	Tantalum cap.	2.2 u	20 % 16 V 3.2x1.6x1.6
C729	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C750	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C751	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C752	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
L103	3203701	Ferrite bead 33r/100mhz	0805	0805
L104	3203701	Ferrite bead 33r/100mhz	0805	0805
L105	3203701	Ferrite bead 33r/100mhz	0805	0805
L106	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L107	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L108	3640035	Filt z>450r/100m 0r7max 0.2a 0603		0603
L500	3645207	Chip coil	56 n	2 % Q=38/200 MHz 0603
L501	3645207	Chip coil	56 n	2 % Q=38/200 MHz 0603
L502	3645055	Chip coil	120 n	2 % Q=50/250 MHz 0805
L503	3645057	Chip coil	82 n	2 % Q=65/500 MHz 0805
L504	3645057	Chip coil	82 n	2 % Q=65/500 MHz 0805
L506	3641546	Chip coil	82 n	10 % Q=40/150 MHz 0805
L507	3641548	Chip coil	100 n	10 % Q=40/150 MHz 0805
L509	3641626	Chip coil	220 n	2 % Q=30/100 MHz 0805
L510	3641626	Chip coil	220 n	2 % Q=30/100 MHz 0805
L511	3645209	Chip coil	33 n	2 % Q=40/250 MHz 0603
L512	3646003	Chip coil	2 n	Q=30/800M 0402
L513	3646003	Chip coil	2 n	Q=30/800M 0402
L516	3645001	Chip coil	4 n	10 % Q=10/100 MHz 0603
L560	3203705	Ferrite bead 0.015r 42r/100m 0805		0805
L561	3645157	Chip coil	100 n	10 % Q=12/100 MHz 0603
L565	3645055	Chip coil	120 n	2 % Q=50/250 MHz 0805
L570	3646005	Chip coil	2 n	Q=29/800M 0402
L601	3641334	Chip coil	270 n	5 % Q=28/25 MHz 1008
L652	3641206	Chip coil		10% Q=25/7.96 MHz 1008
L653	3645157	Chip coil	100 n	10 % Q=12/100 MHz 0603
L654	3645157	Chip coil	100 n	10 % Q=12/100 MHz 0603

L655	3645157	Chip coil	100 n	10 % Q=12/100 MHz 0603
L656	3645129	Chip coil	18 n	5 % Q=8/100M 0603
L657	3645205	Chip coil	22 n	5 % Q=30/800M 0603
L658	3203709	Ferrite bead 0.5r 120r/100m	0402	0402
L659	3203709	Ferrite bead 0.5r 120r/100m	0402	0402
L660	3203709	Ferrite bead 0.5r 120r/100m	0402	0402
L662	3203709	Ferrite bead 0.5r 120r/100m	0402	0402
L663	3203709	Ferrite bead 0.5r 120r/100m	0402	0402
B100	4510159	Crystal	32.768 k	+–20PPM
G550	4350147	Vco 1950–2073mhz 2.8v 10ma		
G650	4510213	VCTCXO	13 M	+–5PPM 2.8V GSM/PCN
G660	4350145	Vco 480mhz 2.8v 7ma 9.0x7.0x1.7		
F100	5119019	SM, fuse f 1.5a 32v	0603	
Z500	4511057	Saw filter	947.5+–12.5 M	/3.6DB 4X4
Z501	4511055	Saw filter	1842.5+–37.5 M	3.1x3.1
Z560	451P010	Use code 4512087		
Z574	4511015	Saw filter	902.5+–12.5 M	/3.8DB 4X4
Z575	4511063	Saw filter	1747.5+–37.5 M	
Z600	4511061	Saw filter	73+–0.09 M	14.2x8.4
Z601	4510009	Cer.filt 13+–0.09mhz	7.2x3.2	7.2x3.2
T500	3640413	Transf balun 1.8ghz+/–100mhz	1206	1206
V100	1825005	Chip varistor vwm14v vc30v	0805	0805
V102	4113651	Trans. supr.	QUAD	6 V SOT23–5
V103	4113601	Emi filter emif01–5250sc5 sot23–5		SOT23–5
V104	4113651	Trans. supr.	QUAD	6 V SOT23–5
V105	4113651	Trans. supr.	QUAD	6 V SOT23–5
V111	4210099	Transistor		SCT595
V112	4219904	Transistor x 2	UMX1	npn 40 V SOT363
V116	4110067	Schottky diode	MBR0520L	20 V 0.5 A SOD123
V250	4210100	Transistor	BC848W	npn 30 V SOT323
V401	4210052	Transistor	DTC114EE	npn RB V EM3
V402	4210102	Transistor	BC858W	pnp 30 V 100 mA 200MWSOT323
V560	4110014	Sch. diode x 2	BAS70–07	70 V 15 mA SOT143
V600	4210132	Transistor		SOT323
D200	4370415	Mad2 rom4 v14 f721727 c10 tqfp176		TQFP176
D210	4340509	IC, flash mem.		TSOP48
D221	4340397	IC, SRAM		STSOP3
D230	4340357	IC, EEPROM		SO8
D402	4340369	IC, dual bus buffer sso	TC7W126FU	SSOP8
N100	4370391	Ccont2h dct3 bb asic	tqfp64	TQFP64
N101	4370165	Chaps charger control	so16	SO16
N201	4340413	IC, regulator	TK11230BMC	3.0 V SOT23L
N250	4370363	Cobba_gj b09 bb asic	tqfp64	TQFP64
N300	4113631	Esd array10 ip401		4CV24–45R SSOP2SSOP24
N400	4860031	Tfdu4100 irda tx/rx>2.7v 115kbits		115KBITS

N500	4370407	Crfu3 rf asic gsm/pcn e1 tqfp–48		TQFP–48
N501	4370451	Rf9117e6 pw amp 890–915mhz		
N502	4370453	Rf9118e6 pw amp 1710–1785mhz edss		EDSS
N600	4370351	Summa v2 rx,tx,pll,pcontr. tqfp48		TQFP48
N620	4340335	IC, regulator	TK11228AM	SSO6
S301	5219005	IC, SWsp–no 30vdc 50ma smSW TACT		SMD
S302	5219005	IC, SWsp–no 30vdc 50ma smSW TACT		SMD
X100	5469061	SM, system conn 6af+3dc+mic+jack		
X101	5469069	SM, batt conn 2pol spr p3.5 100v		100V2A
X102	5469069	SM, batt conn 2pol spr p3.5 100v		100V2A
X300	5460021	SM, conn 2x14m spring p1.0 pcb/p		PCB/PCB
X302	5409033	Sim card reader ccm04–5004 2x3smd		2x3smd
X560	5429007	SM, coax conn m sw 50r 0.4–2ghz		
A510	9517019	Pa–can dmc01137		
	9854212	PCB UG3 123.3X41.0X0.9 M6 4/PA		